EG06 Series

Hardware Design

LTE-A Module Series

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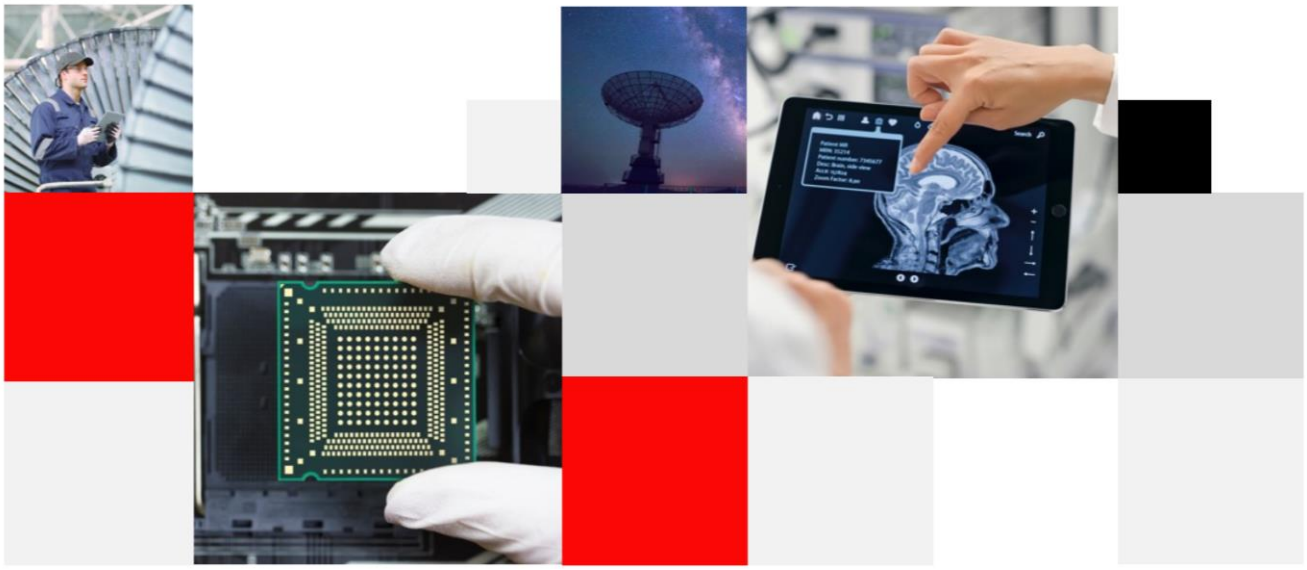

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2018-04-11	King MA/ Wison HE	Initial
1.1	2018-11-01	King MA/ Reed WANG/ Devin CHENG/ Xavier XIA	1. Updated the supported bands of EG06-A in Table 1. 2. Changed pins 91, 197–201 and 209–213 into RESERVED ones. 3. Updated the reference circuit of USB application in Figure 20. 4. Added GNSS performance parameters in Table 28. 5. Updated the current consumption of EG06-E in Table 41. 6. Added Table 42: EG06-A Current Consumption. 7. Updated the conducted RF receiving sensitivity of EG06-E in Table 44. 8. Added Table 45: EG06-A Conducted RF Receiving Sensitivity. 9. Updated the reflow soldering thermal profile and related parameters in Chapter 8.2.
1.2	2021-02-03	King MA/ Archibald JIANG/ Waller GUO	1. Changed pins 77–80 into RESERVED ones. 2. Changed the state of SD card interface into under development. 3. Added the precautions of conflict between main serial port flow control and I2C interface in Chapter 3.12. 4. Updated description of GPIO1 and GPIO2. 5. Added the reuse functions of BT_TXD (pin 163), BT_RXD (pin 165), BT_CTS (pin 164) and BT_RTS (pin 166), which can be reused as SPI interface functions. 6. Changed the zener diode to TVS diode in Figure 9.

			7. Updated the related parameters in Chapter 8.2. 8. Added the RC mode of PCIe in Chapter 3.17.1. 9. Deleted EG06-LA and EG06-EL. Added EG06-EA. 10. Changed pin 152 from RESERVED to I2S_MCLK. 11. Updated the weight in Table 3.
1.3	2021-03-16	Archibald JIANG/ Waller GUO	Added the frequency of LTE B41 in Table 33.

Contents

Table Index

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1 Introduction

This document provides information on the functional features, interface specifications, as well as electrical and mechanical details of the EG06 series modules (EG06-E, EG06-A,EG06-AUTL, EG06-EA). Consult this document to learn about the air and hardware interfaces and external application reference designs among other related information of the series modules.

This document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.

2 Product Concept

2.1. General Description

EG06 is a series of LTE-FDD/LTE-TDD/WCDMA wireless communication modules with receive diversity and provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, and WCDMA networks. It also provides GNSS [1)] and voice functionalities [2)] to meet your specific application demands.

EG06 series contains four variants: EG06-E, EG06-A, EG06-AUTL and EG06-EA. You can choose a dedicated type based on your region or operator(s). The following table shows the frequency bands of the series.

Table 2: Frequency Bands of EG06 Series

Mode	EG06-E	EG06-A	EG06-AUTL	EG06-EA
LTE-FDD (with Rx-diversity)	B1/B3/B5/B7/B8/ B20/B28/B32 [3)]	B2/B4/B5/B7/B12/B13/ B25/B26/B29 [3)]/B30/B66	B3/B7/B28	B1/B3/B5/ B7/B8/B20/ B28/B32 [3)]
LTE-TDD (with Rx-diversity)	B38/B40/B41	Not supported	Not supported	B38/B40/B41
2CA	B1 + B1/B5/B8/ B20/B28; B3 + B3/B5/B7/ B8/B20/B28; B7 + B5/B7/B8/ B20/B28; B20 + B32 [3)]; B38 + B38; B40 + B40; B41 + B41	B2 + B2/B5/B12/ B13/B29 [3)]; B4 + B4/B5/B12/ B13/B29 [3)]; B7 + B5/B7/B12/B26; B25 + B5/B12/B25/B26; B30 + B5/B12/B29 [3)]; B66 + B5/B12/B13 B29 [3)]/B66	B3 + B3/B7/ B28; B7 + B7/B28	B1 + B1/B3/B5/ B7/B8/B20/B28; B3 + B3/B5/B7/ B8/B20/B28; B5 + B5; B7 + B5/B7/B8/ B20/B28; B20 + B32 [3)]; B38 + B38; B40 + B40; B41 + B41
WCDMA (with Rx-diversity)	B1/B3/B5/B8	B2/B4/B5	Not supported	B1/B3/B5/B8

GNSS	GPS, GLONASS, BeiDou, Galileo, QZSS	GPS, GLONASS, BeiDou, Galileo, QZSS	GPS, GLONASS, BeiDou, Galileo, QZSS	GPS, GLONASS, BeiDou, Galileo, QZSS

NOTES

1. [1)] The GNSS function is optional.
2. [2)] EG06 series modules (EG06-E/EG06-A/EG06-AUTL/EG06-EA) come in two versions: **Telematics** and **Data-only**; The former supports voice and data functions while the latter only data function.
3. [3)] B32 and B29 support Rx only, and in 2CA, they are only for secondary component carrier.

With a compact profile of 37.0 mm × 39.5 mm × 2.8 mm, EG06 series can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EG06 is a series of SMD-type modules which can be embedded in applications through its 299 LGA pins.

2.2. Key Features

The following table describes the detailed features of the module.

Table 3: Key Features of EG06 series

Feature	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 3 (24 dBm +1/-3 dB) for WCDMA bands ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	● Support up to Cat 6 FDD and TDD CA ● Support uplink QPSK and 16QAM modulation ● Support downlink QPSK, 16QAM and 64QAM modulation ● Support 1.4 MHz to 40 MHz (DL 2CA) RF bandwidth ● Support 2 × 2 MIMO in DL direction FDD: Max. 300 Mbps (DL)/50 Mbps (UL) TDD: Max. 226 Mbps (DL)/28 Mbps (UL)
UMTS Features	● Support 3GPP R8 DC-HSDPA, HSPA + HSDPA, HSUPA and WCDMA

	● Support QPSK, 16QAM and 64QAM modulation DC-HSDPA: Max. 42 Mbps (DL) HSUPA: Max. 5.76 Mbps (UL) WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
Internet Protocol Features	Support QMI/FTP/HTTP/NTP/PING/HTTPS/ protocols
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Support (U)SIM card: 1.8/3.0 V
Audio Features	● Support one digital audio interface: PCM interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec ● Support 16-bit linear data format ● Support long frame synchronization and short frame synchronization ● Support master and slave modes, but must be the master in long frame synchronization
USB Interface	● Comply with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice over USB*. ● Support USB serial drivers for: Windows 7/8/8.1/10; WinCE 5.0/6.0/7.0*; Linux 2.6/3.x/4.1–4.14; Android 4.x/5.x/6.x/7.x/8.x.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate reaches up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	● Gen8C-Lite of Qualcomm ● Protocol: NMEA 0183
AT Commands	Comply with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status

Antenna Interfaces	Including a Main antenna interface (ANT_MAIN), a Rx-diversity antenna interface (ANT_DIV) and a GNSS antenna interface (ANT_GNSS).
Physical Characteristics	● Size: (37.0 ±0.15) mm × (39.5 ±0.15) mm × (2.8 ±0.2) mm ● Weight: approx. 9.1 g
Temperature Range	● Operating temperature range: -35 to + 75 °C [1)] ● Extended temperature range: -40 to + 85 °C [2)] ● Storage temperature range: -40 to + 90 °C
Firmware Upgrade	USB interface and DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module keeps the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There will not be unrecoverable malfunctions. Nor will there be effects on the radio spectrum or harm to radio networks. Only one or more parameters like P_{out} might reduce in the value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
3. When CTS (pin 56) and RTS (pin 57) of the main serial port are used for flow control, I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface cannot be used for I2C functions.
   When I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface are used for I2C functions, CTS (pin 56) and RTS (pin 57) of the main serial port cannot be used as flow control.

2.3. Functional Diagram

Below is the block diagram of EG06 series with its major functional parts illustrated.

- Power management
- Baseband
- DDR + NAND flash memory
- Radio frequency
- Peripheral interfaces

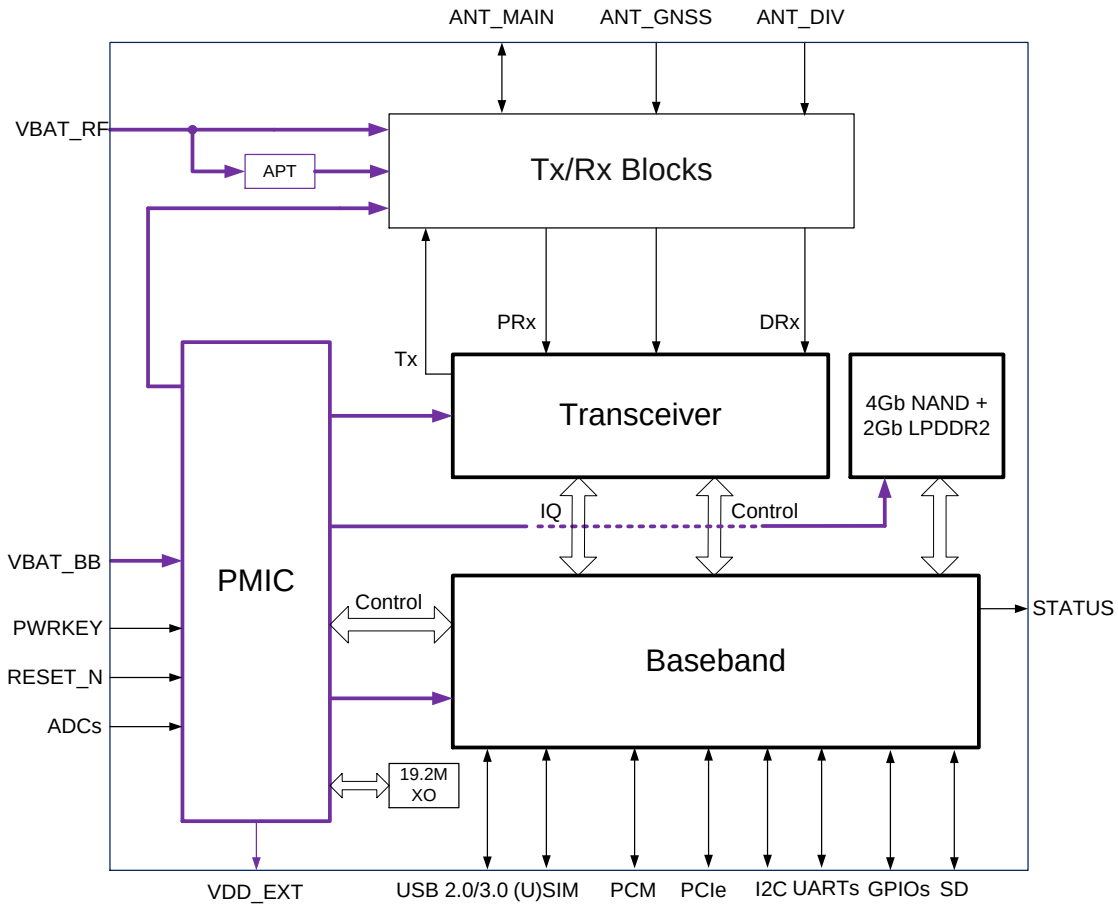


Figure 1: Functional Diagram

2.4. Evaluation Board

To help you develop applications handily with EG06 Series, Quectel supplies an evaluation board (EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EG06 series is equipped with 299 LGA pins that can connect to a cellular application platform. Sub-interfaces of the series are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- ADC interfaces
- Network Indication Interface
- Module STATUS indication Interface
- RI Behaviors
- PCIe interface*
- WLAN control interface*
- SD card interface*
- USB_BOOT interface
- SPI Interface

3.2. Pin Assignment

The following figure shows the pin assignment of EG06 series.

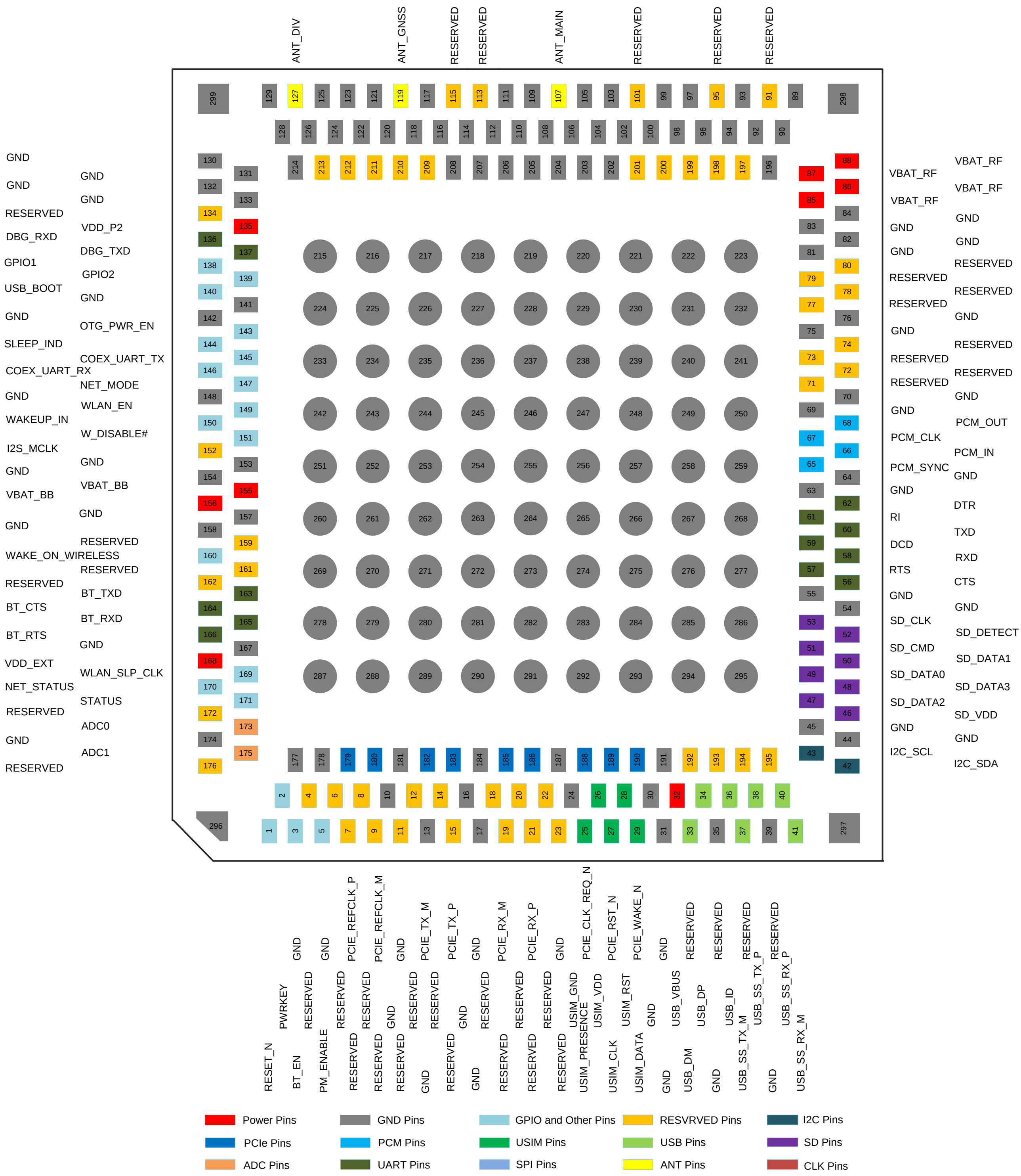


Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins 215–299 should be connected to ground in the design.

3.3. Pin Description

The following tables define and describe the pins of EG06 series.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
DIO	Digital Input/Output
OD	Open drain
PI	Power input
PO	Power output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be able to provide a sufficient current of 0.8 A at least.
VBAT_RF	85, 86, 87, 88	PI	Power supply for the module's RF	Vmax = 4.3 V Vmin = 3.3 V	It must be able to provide a sufficient

			part	Vnom = 3.8 V	current of at least 1.2 A in a transmitting burst.
VDD_EXT	168	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits.
VDD_P2	135	PI	It is determined by external circuit		If an SD card is used, connect VDD_P2 to SD_VDD. If no SD card is used, connect VDD_P2 to VDD_EXT.
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114, 116, 117, 118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191,196, 202–208, 214–299				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	2	DI	Turn on/off the module	V_{IH}max = 2.1 V V_{IH}min = 0.8 V V_{IL}max = 0.5 V	The output voltage is 0.8 V because it is pulled up to an internal voltage (800 mV).
RESET_N	1	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	171	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_MODE	147	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_STATUS	170	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	32	PI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	
USB_DP	34	DIO	USB differential data (+)	Compliant with USB 2.0 standard specifications.	Require a differential impedance of 90 Ω.
USB_DM	33	DIO	USB differential data (-)	Compliant with USB 2.0 standard specifications.	
USB_ID*	36	DI	USB ID detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)	Compliant with USB 3.0 standard specifications.	Require differential impedance of 90 Ω.
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)		
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)		Require a differential impedance of 90 Ω.
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)		
OTG_PWR_EN*	143	DO	OTG power control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	24		Specified ground for (U)SIM card		
USIM_VDD	26	PO	(U)SIM card power supply	**For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.75 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically.

USIM_DATA	29	DIO	(U)SIM card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.36 V V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.45 V **For 3.0 V (U)SIM:** V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_CLK	27	DO	(U)SIM card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.45 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_RST	28	DO	(U)SIM card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.45 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_ PRESENCE	25	DI	(U)SIM card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	61	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DCD	59	DO	Data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CTS	56	DO	Clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RTS	57	DI	Request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep it

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	open.
DTR	62	DI	Data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Pulling it down to low level will wakes up the module. If unused, keep it open.
TXD	60	DO	Transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RXD	58	DI	Receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
BT UART Interface* (Can be multiplexed into SPI interface)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_TXD	163	DO	BT UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MOSI.
BT_RXD	165	DI	BT UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MISO.
BT_RTS	166	DI	BT UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_CS.
BT_CTS	164	DO	BT UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.

					BT UART interface pin by default. Can be multiplexed into SPI_CLK.
BT_EN	3	DO	BT function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Keep it open. This function is under development.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	136	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	137	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General-purpose ADC interface	Voltage range: 0.15 V to VBAT_BB	If unused, keep it open.
ADC1	175	AI	General-purpose ADC interface	Voltage range: 0.15 V to VBAT_BB	If unused, keep it open.
PCM and I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	66	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	65	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal.

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep it open.
PCM_CLK	67	DIO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C_SCL	43	OD	I2C serial clock (for external codec)	1.8 V power domain	An external pull-up resistor is required. 1.8 V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data (for external codec)	1.8 V power domain	An external pull-up resistor is required. 1.8 V only. If unused, keep it open.
I2S_MCLK	152	DO	Clock output		Provide a digital clock output for an external audio codec. If unused, keep it open
PCIe Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)		If unused, keep it open.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)		If unused, keep it open.
PCIE_TX_M	182	AO	PCIe transmit (-)		If unused, keep it open.
PCIE_TX_P	183	AO	PCIe transmit (+)		If unused, keep it open.
PCIE_RX_M	185	AI	PCIe receive (-)		If unused, keep it open.
PCIE_RX_P	186	AI	PCIe receive (+)		If unused, keep it open.
PCIE_CLKREQ_N	188	DIO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it

				V_{IH}max = 2.0 V	open.
PCIE_RST_N	189	DIO	PCIe reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE_N	190	DIO	PCIe wake up	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V V_{IH}max = 2.0 V	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PM_ENABLE	5	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	Wake up the host by a Wi-Fi module.	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active low. If unused, keep it open.
WLAN_EN	149	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. If unused, keep it open.
COEX_UART_RX	146	DI	LTE&WLAN coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
COEX_UART_TX	145	DO	LTE&WLAN coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If unused, keep it open.
SD Card Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SD_VDD	46	PO	SDIO power supply	**For 1.8 V SD:** Vmax = 1.9 V Vmin = 1.75 V **For 3.0 V SD:** Vmax = 3.05 V Vmin = 2.75 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically. Power supply of SD card must be provided by an external power supply.
SD_DATA0	49	DIO	SDIO data bit 0	**For 1.8 V SD:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.3 V V_{IH}max = 2.0 V **For 3.0 V SD:** V_{OL}max = 0.35 V V_{OH}min = 2.15 V V_{IL}min = -0.3 V V_{IL}max = 0.7 V V_{IH}min = 1.8 V V_{IH}max = 3.15 V	If unused, keep it open.
SD_DATA1	50	DIO	SDIO data bit 1		If unused, keep it open.
SD_DATA2	47	DIO	SDIO data bit 2		If unused, keep it open.
SD_DATA3	48	DIO	SDIO data bit 3		If unused, keep it open.
SD_CMD	51	DIO	SDIO command		If unused, keep it open.
SD_CLK	53	DO	SDIO clock		If unused, keep it open.
SD_DETECT	52	DI	SD card detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	127	AI	Diversity antenna interface		50 Ω impedance. If unused, keep it open.
ANT_MAIN	107	DIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	119	AI	GNSS antenna interface		50 Ω impedance. If unused, keep it open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

WAKEUP_IN	150	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. Driving it to low level wakes up the module. If unused, keep it open.
W_DISABLE#	151	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. In low voltage level, the module can enter airplane mode. If unused, keep it open.
GPIO1	138	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If unused, keep them open.
GPIO2	139	DIO			
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	140	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SLEEP_IND	144	DO	Indicate the module's sleep mode	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	4, 6, 7, 8, 9, 11, 12, 14, 15, 18–23, 71–74, 77–80, 91, 95, 101, 113, 115, 134, 159, 161, 162, 172, 176, 192–195, 197–201, 209–213				Keep these pins unconnected.

NOTES

1. When CTS (pin 56) and RTS (pin 57) of the main serial port are used for flow control, I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface cannot be used for I2C functions.
   When I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface are used for I2C functions, CTS (pin 56) and RTS (pin 57) of the main serial port cannot be used for flow control.
2. BT_TXD (pin 163), BT_RXD (pin 165), BT_CTS (pin 164) and BT_RTS (pin 166) can be multiplexed into SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CS respectively. See ***Chapter 3.21*** for details. SPI

interface and BT UART interface cannot be used at the same time; only one of them can be used at a time.
3. If an SD card is used, connect VDD_P2 (pin 135) to SD_VDD (pin 46). If no SD card is used, connect VDD_P2 (pin 135) to VDD_EXT (pin 168).
4. GPIO1 (pin 138) and GPIO2 (pin 139) are dedicated for external tuner control.

3.4. Operating Modes

The table below briefly summarizes various operating modes referred in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	The module has registered on network and is ready to send and receive data, its software being active.
	Talk/Data	The module is connected to network, its power consumption decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module into minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module into airplane mode where the RF function is invalid.	
Sleep Mode	The module keeps receiving paging messages, SMS, voice calls and TCP/UDP data from the network, its current consumption reduced to the minimal level.	
Power Down Mode	The module's power supply is cut off by its power management unit, its software being inactive and serial interfaces inaccessible while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

In the sleep mode, DRX, whose cycle index value is broadcasted via the wireless network, reduces the module's current consumption to a minimum level. The figure below shows the relationship between DRX run time and current consumption in this mode: the longer the DRX runs, the lower the current consumption.

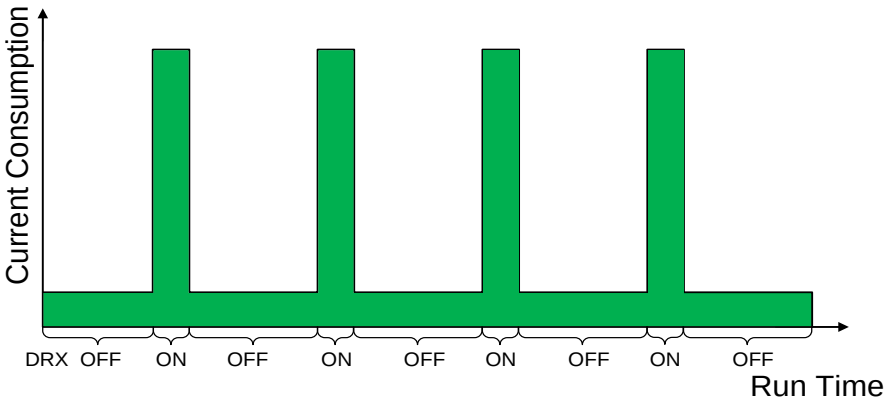


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following sections describe the setup of power saving mode of EG06 in different circumstances.

3.5.1.1. Set Sleep Mode via UART

If the host communicates with the module via UART interface, the following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between module and host in this case.

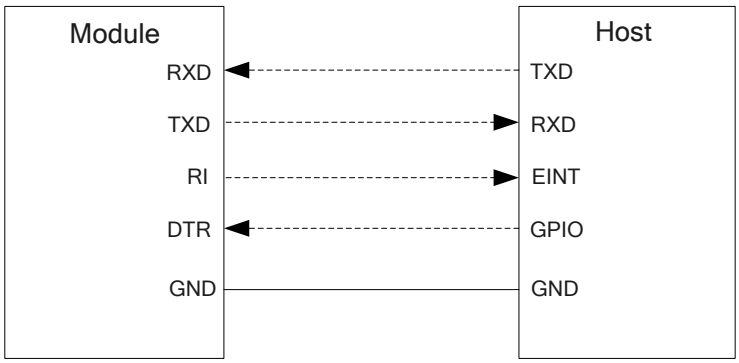


Figure 4: Set Sleep Mode via UART

- Driving the host DTR to low level will wake up the module.
- When the module has a URC to report, an RI signal will wake up the host. See ***Chapter 3.16*** for details about RI behavior.

3.5.1.2. Via USB with Suspend/Resume & Remote Wakeup Functions

If the host supports USB suspend/resume and remote wakeup functions, the following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected to the module's USB interface, is in suspend state.

The following figure shows the connection between module and host in this case.

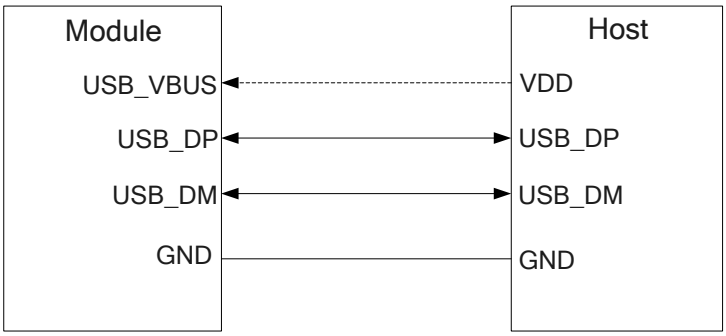


Figure 5: Sleep Mode with USB Remote Wakeup

The module/host will be woken up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals to USB bus to wake up the host.

3.5.1.3. Via USB with Suspend/Resume and RI Functions

If the host supports USB suspend/resume but not remote wake-up, an RI signal is needed to wake up the host.

The following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected to the module's USB interface, is in suspend state.

The following figure shows the connection between module and host in this case.

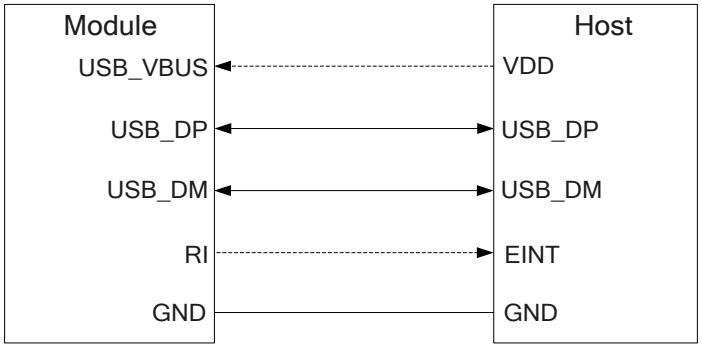


Figure 6: Sleep Mode with RI Signal Wakeup

The module/host will be woken up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, an RI signal will wake up the host.

3.5.1.4. Via USB without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected from an external control circuit to set the module into sleep mode. The following steps are required.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between module and host in this case.

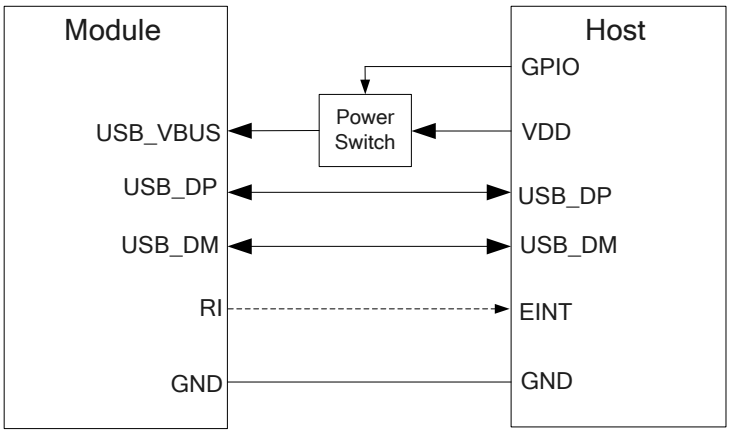


Figure 7: Sleep Mode without Suspend Function

Supplying power to USB_VBUS with the power switch will wake up the module.

NOTE

Please pay attention to the level matching between module and host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF stops working, and all AT commands correlative with RF function are inaccessible. This mode can be set with the following approaches.

Hardware approach:

The W_DISABLE# pin is pulled up by default; driving it low will enable the module to enter airplane mode.

Software approach:

AT+CFUN command provides the choices of functionality level through setting **<fun>** to 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode; RF function is disabled.

NOTES

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by executing **AT+QCFG="airplanecontrol"** command, which is under development.
2. The execution of **AT+CFUN** command will not affect the module's GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG06 series provides six VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for these pins.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86, 87, 88	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for the module's baseband part	3.3	3.8	4.3	V
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114, 116, 117, 118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299		-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage never drops below 3.3 V. The following figure shows the voltage drop in case of burst transmission in 3G and 4G networks.

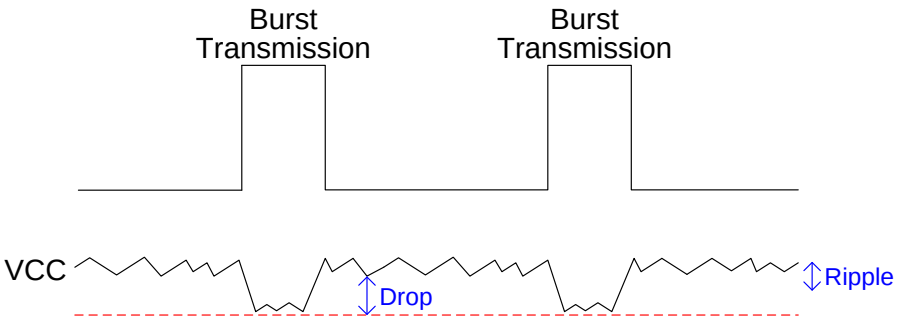


Figure 8: Voltage Drop Limits during Tx

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR should be used, so does a multi-layer ceramic chip (MLCC) capacitor array for its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be the single voltage source which can supply power along two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is recommended to use a TVS diode with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP}. The following figure shows the star structure of the power supply.

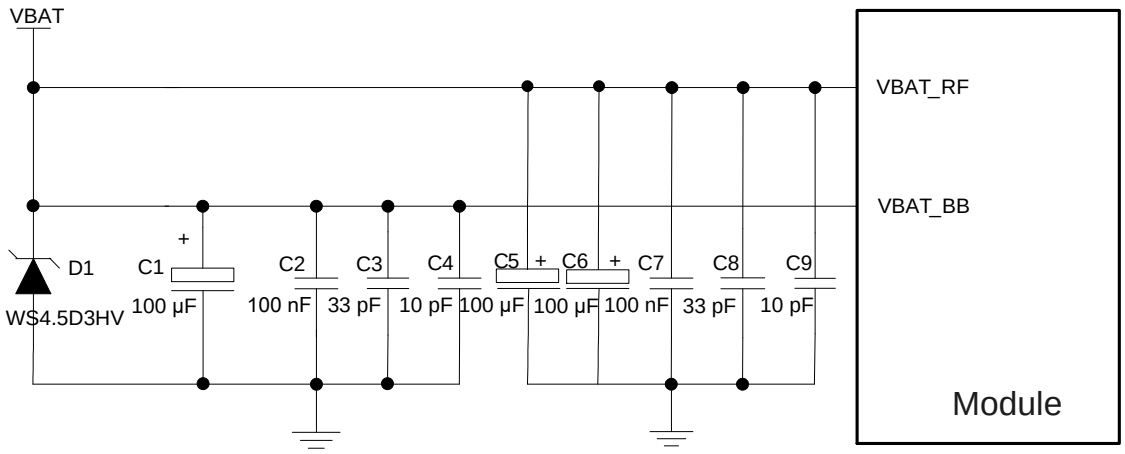


Figure 9: Star Structure of the Power Supply

3.6.3. Reference Design of Power Supply

Power design is critical as the performance of the module largely depends on the stability and suitability of its power source. The power supply of EG06 series should be able to provide a sufficient current of 2 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used while supplying power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for a +5 V input power source. The designed output of the power supply is about 3.8 V and the maximum load current is 3 A.

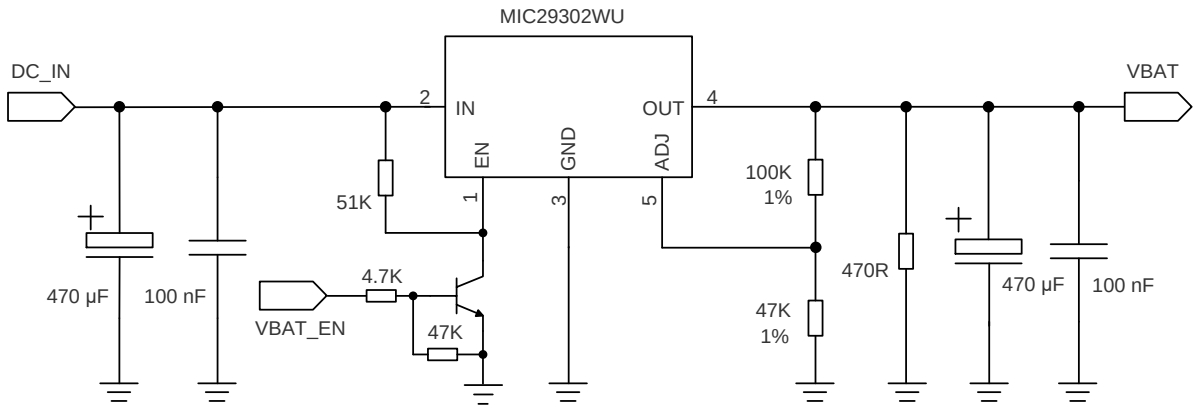


Figure 10: Reference Design of Power Supply

NOTE

To avoid damaging internal flash, please do not switch off power supply when the module works normally. Only after the module is shut down with PWRKEY or AT command can the power supply be cut off.

3.6.4. Monitor the Power Supply

The **AT+CBC** command can be used to monitor the voltage of VBAT_BB. For more details, see ***document [1]***.

3.7. Turn on/off

3.7.1. Turn on the Module with PWRKEY

Table 8: Pin Description of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	2	Turn on/off the module	V_{IH}max = 2.1 V V_{IH}min = 0.8 V V_{IL}max = 0.5 V	The output voltage is 0.8 V because it is pulled up to an internal voltage (800 mV).

When EG06 Series is in power down mode, you can set the module into normal mode by driving the PWRKEY pin to a low level for at least 500 ms, advisably using an open collector driver, before releasing it after the STATUS pin outputs high level. A reference design is given below.

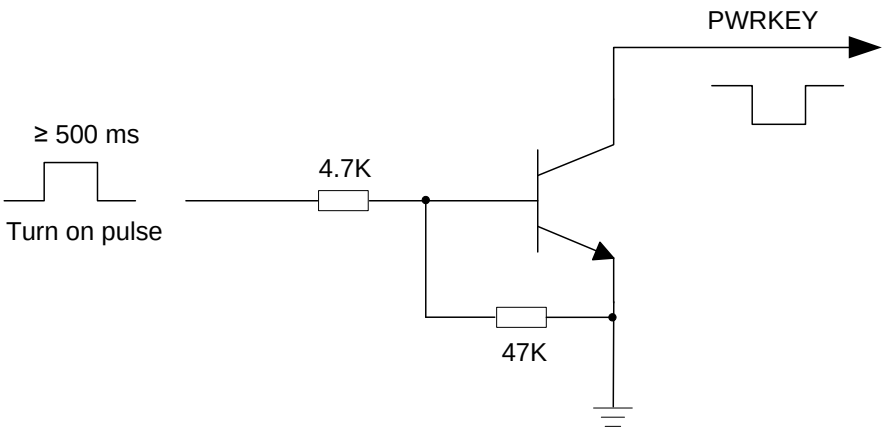


Figure 11: Turn on the Module with Driving Circuit

Another way to control PWRKEY is by using a button. When you press the key, your fingers may generate electrostatic strikes. Therefore, a TVS component placed near the button for ESD protection is indispensable. A reference design is given below.

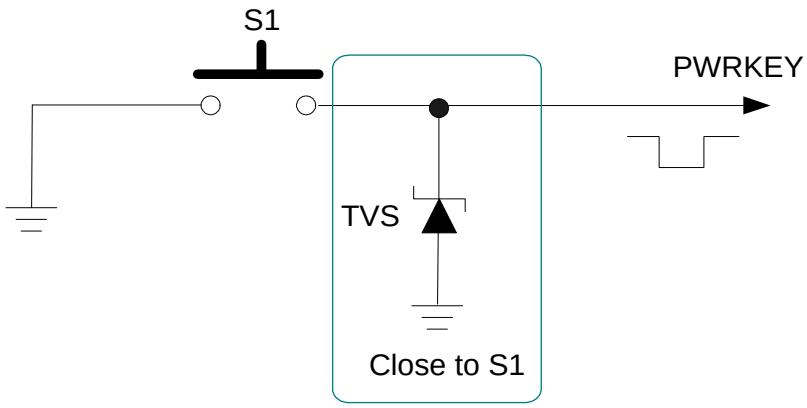


Figure 12: Turn on the Module with Button

The timing of turning on is illustrated in the following figure.

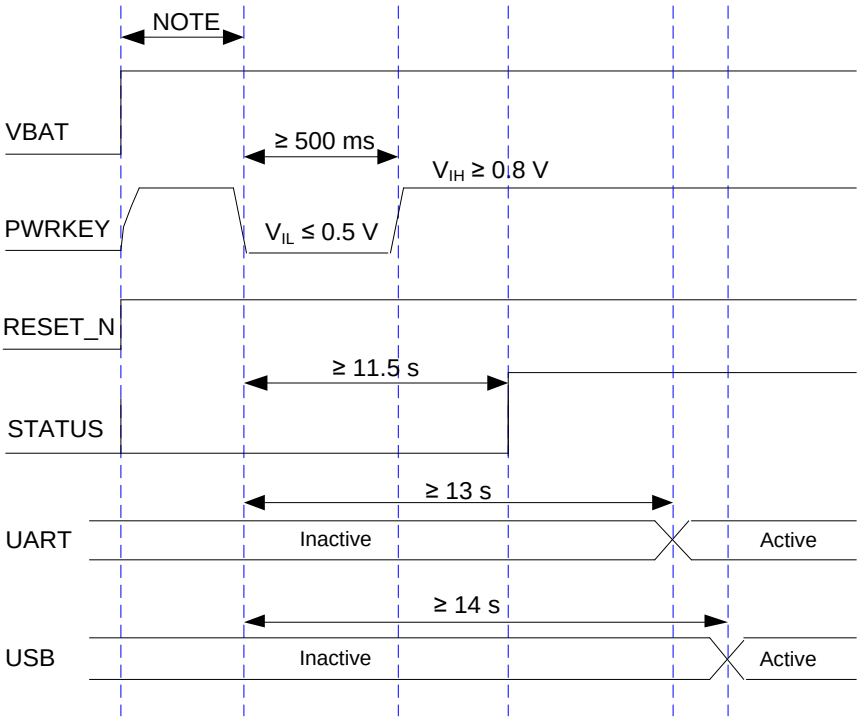


Figure 13: Timing of Turning on the Module

NOTE

Make sure that VBAT is stable for no less than 30 ms before pulling down the PWRKEY pin.

3.7.2. Turn off the Module

Normally, there are two approaches to turning off the module:

- Turn off the module with PWRKEY pin.
- Turn off the module by executing **AT+QPOWD** command.

3.7.2.1. Turn off the Module with PWRKEY

Drive PWRKEY to low level for at least 800 ms, and the module will execute turn-off procedure after the pin is released. The turn-off scenario is illustrated in the following figure.

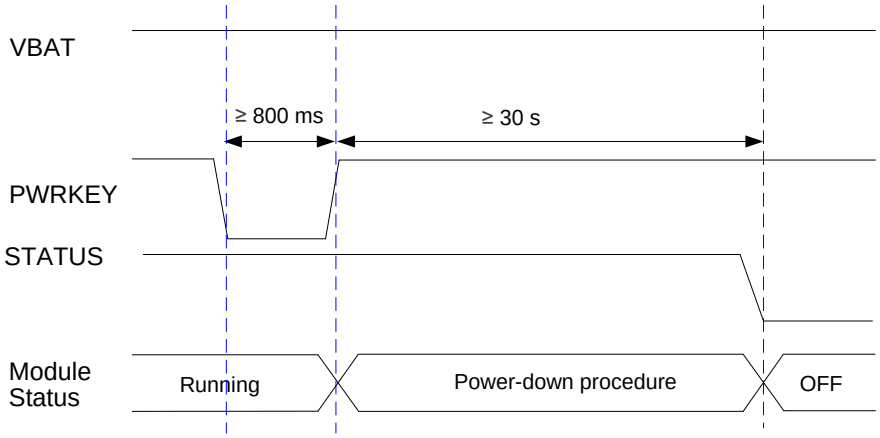


Figure 14: Timing of Turning off the Module

3.7.2.2. Turn off the Module with AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via the PWRKEY pin.

See ***document [1]*** for details about **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down with PWRKEY or **AT+QPOWD** can the power supply be cut off.
2. When turning off the module with **AT+QPOWD**, please keep PWRKEY at high level after executing the power-off command. Otherwise, the module will turn on again after being turn off.

3.8. Reset the Module

The module can be reset by driving the RESET_N LOW for 250–600 ms.

Table 9: Pin Description of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	1	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

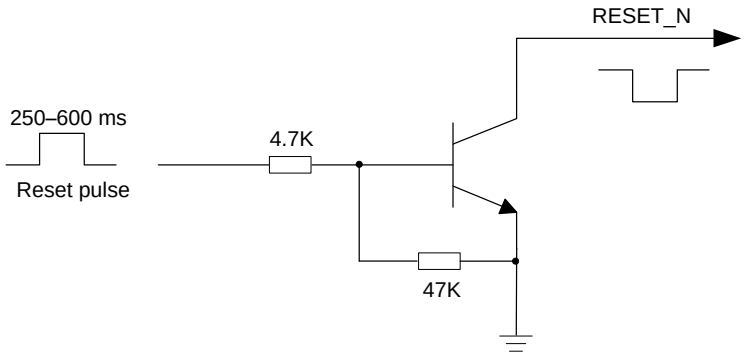


Figure 15: Resetting the Module with Driving Circuit

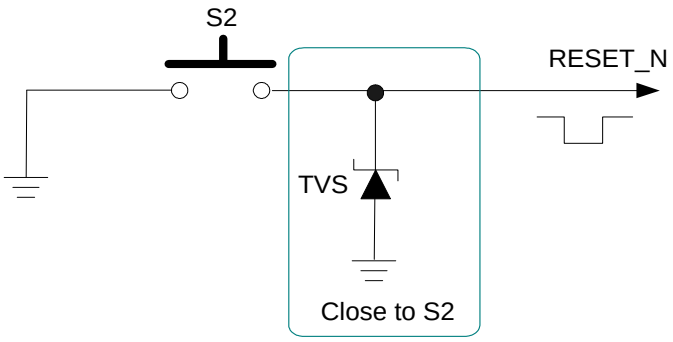


Figure 16: Resetting the Module with Button

The timing of reset is illustrated in the following figure.

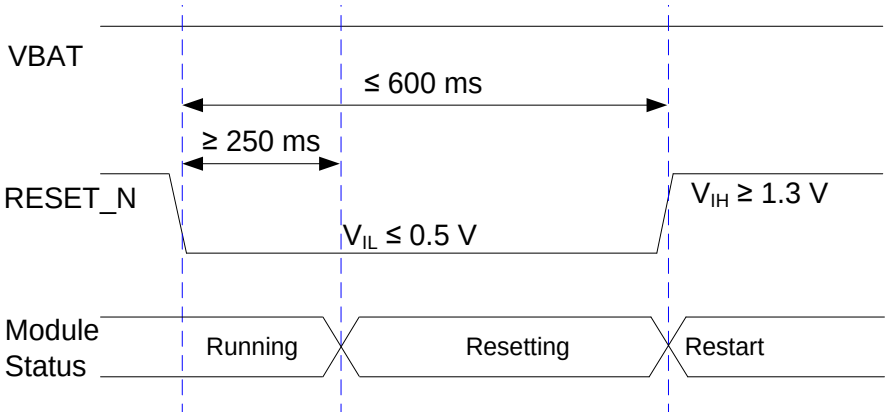


Figure 17: Timing of Resetting the Module

NOTES

1. Reset the module with RESET_N only when it fails to be turned off with **AT+QPOWD** or PWRKEY.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM cards is supported.

Table 10: Pin Definition of the (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	26	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	29	DIO	(U)SIM card data	
USIM_CLK	27	DO	(U)SIM card clock	
USIM_RST	28	DO	(U)SIM card reset	
USIM_PRESENCE	25	DI	(U)SIM card insertion detect	
USIM_GND	24		Specified ground for (U)SIM card	

The module supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, which is disabled by default. See ***document [1]*** about **AT+QSIMDET** command for details.

Below is a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

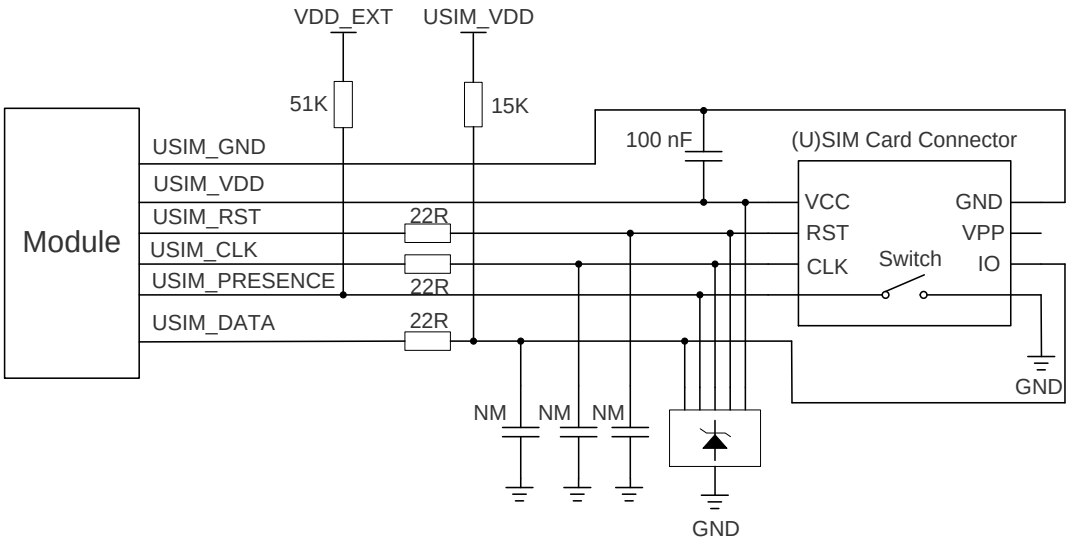


Figure 18: Reference Design of (U)SIM Interface with 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE disconnected. A reference design for (U)SIM interface with a 6-pin (U)SIM card connector is shown below.

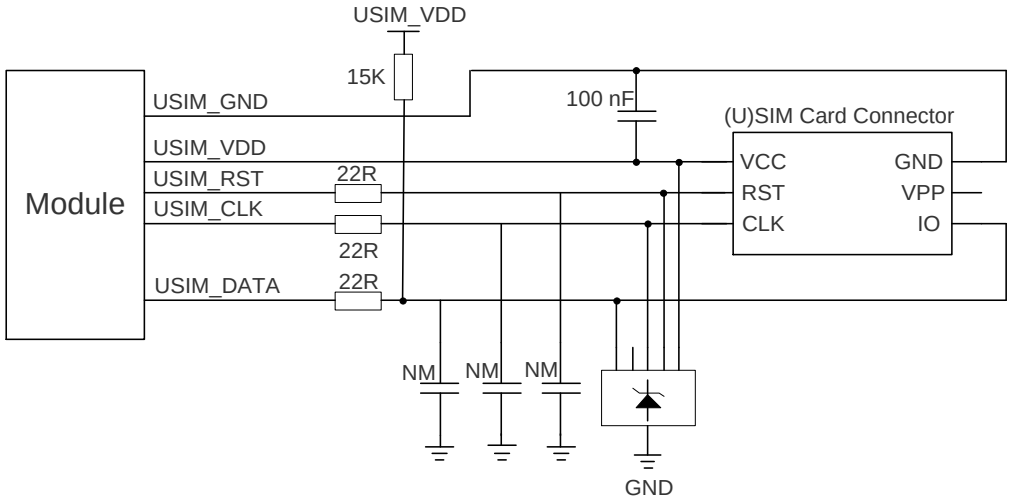


Figure 19: Reference Design of (U)SIM Interface with 6-Pin (U)SIM Card Connector

In order to enhance the reliability and usability of the (U)SIM card in use, please follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make the ground between module and (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to avoid any decrease in electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should be no more than 50 pF. To facilitate debugging, add 22 Ω resistors in series between module and (U)SIM card. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability in sensitive occasions or when long traces are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG06 series provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0/2.0 specifications and supports super speed (5 Gbps) on USB 3.0, high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	34	DIO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	33	DIO	USB differential data (-)	
USB_VBUS	32	PI	USB connection detect	Typical 5.0 V
USB_ID*	36	DI	USB ID detect	
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)	Require differential impedance of 90 Ω
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)	
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)	Require differential impedance of 90 Ω
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)	
OTG_PWR_EN*	143	DO	OTG power control	

GND	35	Ground

For more details about the USB 2.0 & 3.0 specifications, visit http://www.usb.org/home.

It is recommended to reserve the USB interface in your designs for firmware upgrades. Below is a reference design of USB 2.0 & USB 3.0 interface.

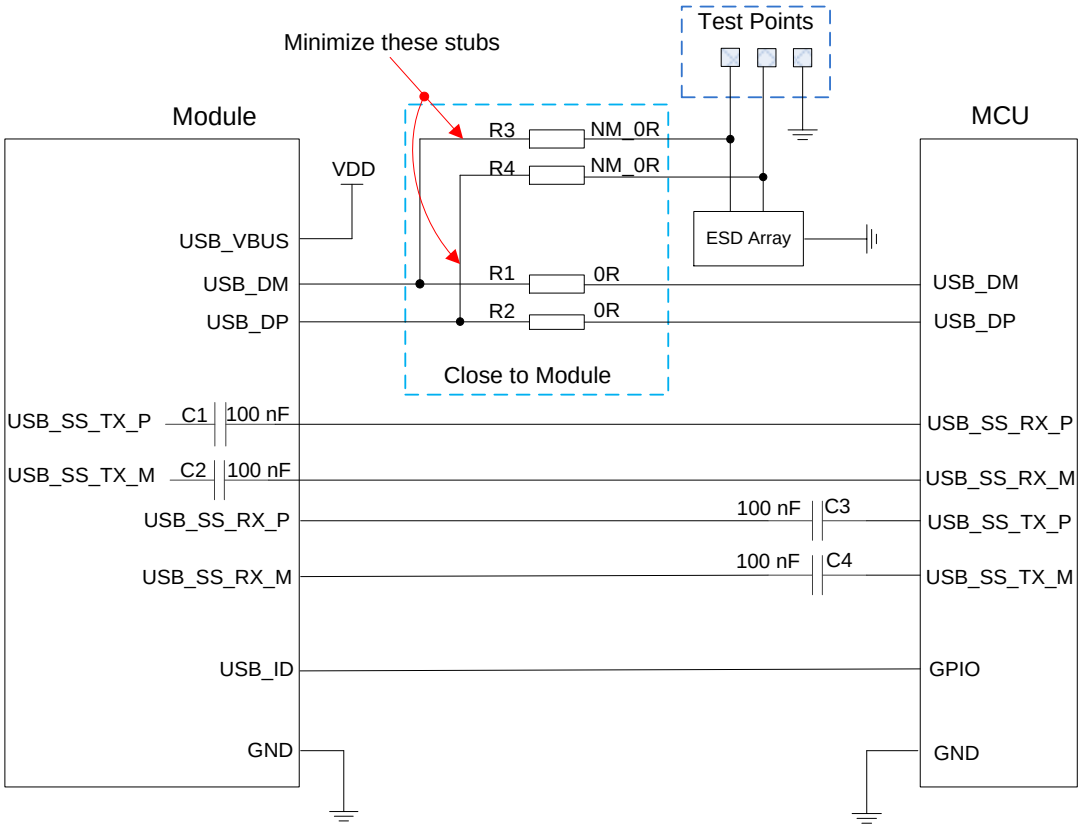


Figure 20: Reference Design of USB Interface

In order to ensure the signal integrity of USB data lines, C1 and C2 have been placed inside the module, C3 and C4 should be placed close to the MCU. R1, R2, R3 and R4 should be placed close to each other and to the module. The extra stubs of trace must be as short as possible.

To meet USB 2.0 & USB 3.0 specifications, the following principles should be complied with while designing the USB interface.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of the differential pairs is 90 Ω.
- For USB 3.0 routing traces, the length difference of Tx and Rx differential pairs should be less than 0.7 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on

the same layer and with ground planes on adjacent layers above and below.

- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2.0 pF for USB 2.0 and less than 0.4 pF for USB 3.0.
- Keep the ESD protection components as close to the USB connector as possible.
- If possible, reserve a 0 Ω resistor on both USB_DP and USB_DM lines.

3.11. UART Interfaces

The module provides three UART interfaces: the main UART interface, the debug UART interface, and the BT UART interface. Their features are shown below:

- The main UART interface supports the following baud rates: 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps, and the default baud rate is 115200 bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.
- The BT UART interface supports 115200 bps baud rate. It is used for BT communication.

Table 12: Pin Definition of the Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	61	DO	Ring indication	1.8 V power domain
DCD	59	DO	Data carrier detect	1.8 V power domain
CTS	56	DO	Clear to send	1.8 V power domain
RTS	57	DI	Request to send	1.8 V power domain
DTR	62	DI	Data terminal ready	1.8 V power domain
TXD	60	DO	Transmit	1.8 V power domain
RXD	58	DI	Receive	1.8 V power domain

NOTES

1. When CTS (pin 56) and RTS (pin 57) of the main serial port are used for flow control, I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface cannot be used for I2C functions.
2. When I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface are used for I2C functions, CTS

(pin 56) and RTS (pin 57) of the main serial port cannot be used for flow control.

Table 13: Pin Definition of the Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	137	DO	Debug UART transmit	1.8 V power domain
DBG_RXD	136	DI	Debug UART receive	1.8 V power domain

Table 14: Pin Definition of the BT UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_TXD	163	DO	BT UART transmit	1.8 V power domain
BT_RXD	165	DI	BT UART receive	1.8 V power domain
BT_CTS	164	DO	BT UART clear to send	1.8 V power domain
BT_RTS	166	DI	BT UART request to send	1.8 V power domain

The module provides 1.8 V UART interfaces. A level translator should be used if the application is equipped with a 3.3 V UART interface. The level translator TXS0108EPWR provided by Texas Instruments is recommended. The reference design is shown below

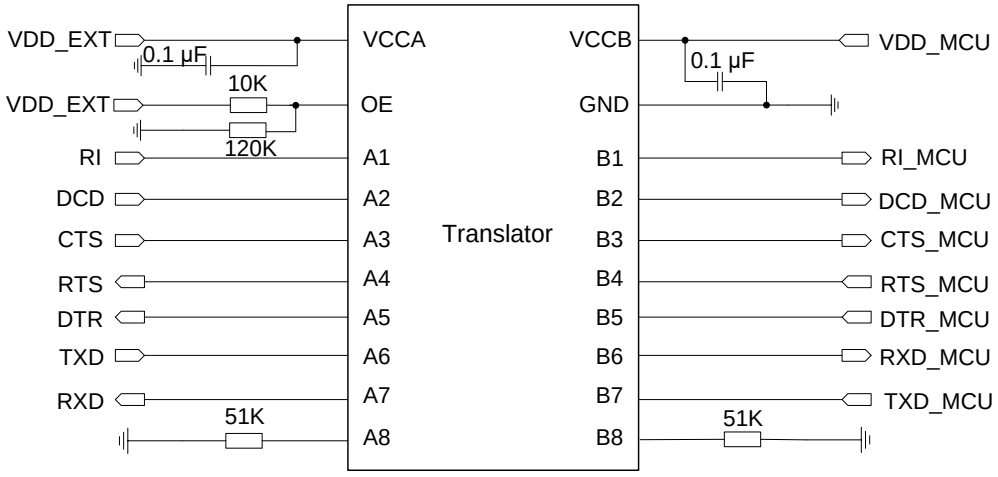


Figure 21: Reference Design of Translator Chip

Please visit http://www.ti.com for more information.

Another approach to level translation is with a transistor circuit. A reference design in this regard is shown below. For the design of circuits shown by dotted lines, both input and output circuit designs, refer to the circuits shown by the solid lines, but pay attention to the direction of connection.

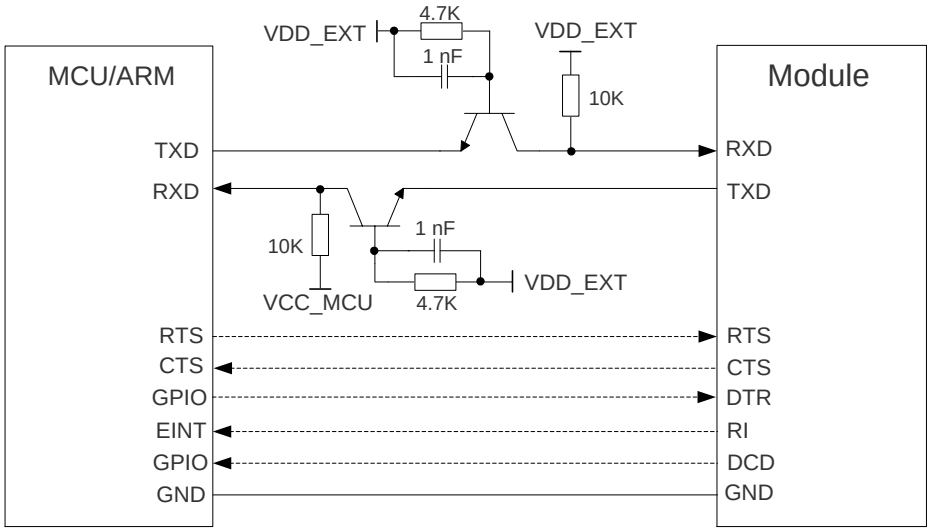


Figure 22: Reference Design of Transistor Circuit

NOTES

1. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module CTS and RTS are connected to the host CTS and RTS respectively.

3.12. PCM and I2C Interfaces

EG06 series supports audio communication via its Pulse Code Modulation (PCM) digital interface and I2C interface.

The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave;
- Auxiliary mode (long frame synchronization): the module works as master only.

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz PCM_SYNC with 50 % duty cycle only.

The module supports 16-bit linear data format. The following figures show the timing relationship between 8 kHz PCM_SYNC and 2048 kHz PCM_CLK in the primary mode as well as that between 8 kHz PCM_SYNC and 256 kHz PCM_CLK in the auxiliary mode.

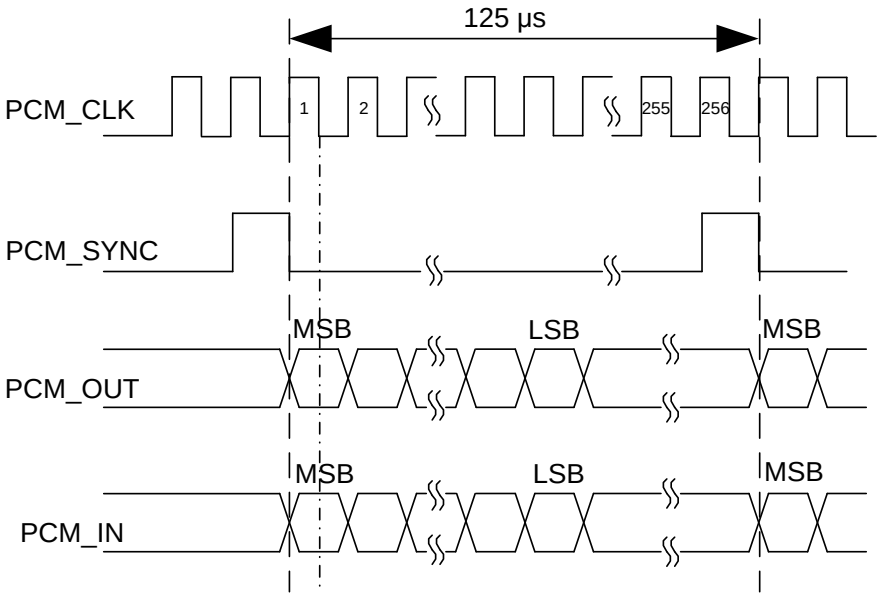


Figure 23: Primary Mode Timing

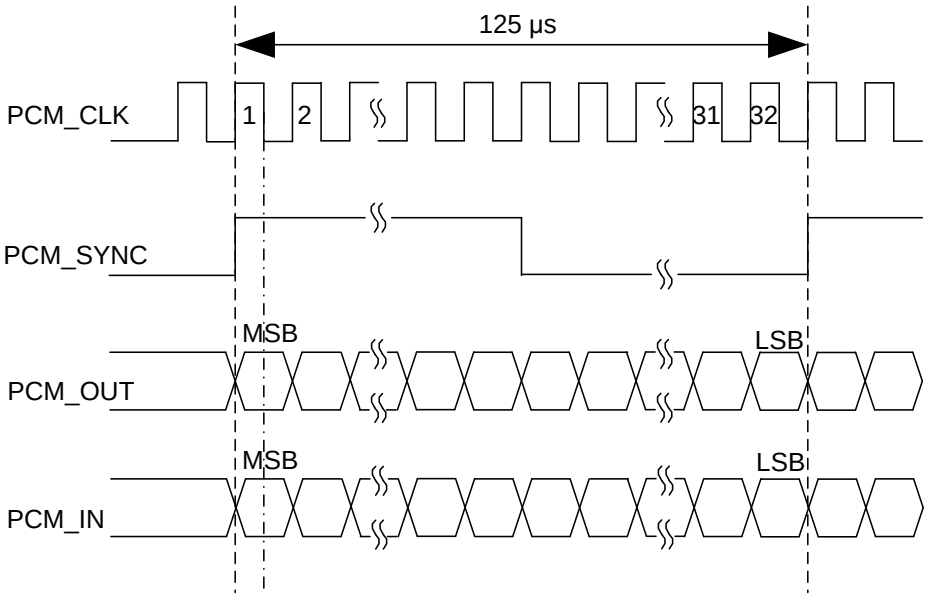


Figure 24: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied to audio codec design.

Table 15: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	66	DI	PCM data input	1.8 V power domain. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	1.8 V power domain. If unused, keep it open.
PCM_SYNC	65	DIO	PCM data frame sync	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	67	DIO	PCM clock	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C_SCL	43	OD	I2C serial clock (for external codec)	Require an external pull-up to 1.8 V
I2C_SDA	42	OD	I2C serial data (for external codec)	Require an external pull-up to 1.8 V
I2S_MCLK	152	DO	Clock output	Provide a digital clock output for an external audio codec. If unused, keep it open.

Clock and mode can be configured by **AT+QDAI**, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [1]*** for details about **AT+QDAI** command.

NOTES

1. When I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface are used for I2C functions, CTS (pin 56) and RTS (pin 57) of the main serial port cannot be used for flow control.
2. When CTS (pin 56) and RTS (pin 57) of the main serial port are used for flow control, I2C_SDA (pin 42) and I2C_SCL (pin 43) of the I2C interface cannot be used for I2C functions.

The following figure shows a reference design of PCM interface with an external codec IC.

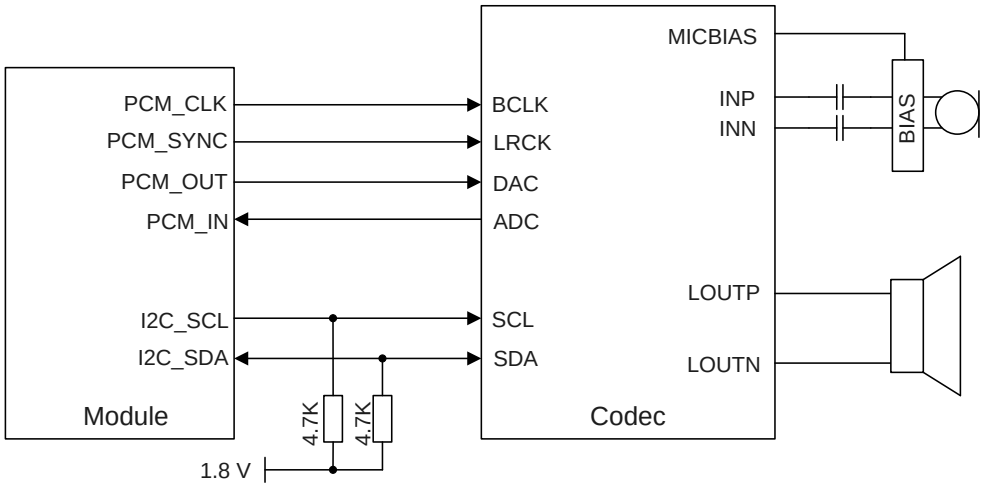


Figure 25: Reference Design of PCM Interface with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG06 series works as the master device pertaining to I2C interface.

3.13. ADC Interfaces

The module provides two Analog-to-Digital Converters (ADC) interfaces. You can execute **AT+QADC=0** to read the voltage value on ADC0 and **AT+QADC=1** to read the voltage value on ADC1. For more details about these **AT+QADC** commands, see ***document [1]***.

To improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 16: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	173	General-purpose ADC interface
ADC1	175	General-purpose ADC interface

Table 17: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.15	-	VBAT_BB	V
ADC1 Voltage Range	0.15	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTES

1. The input voltage of ADC should not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use a resistor divider for ADC application.

3.14. Network Indication Interface

The network indication pins, NET_MODE and NET_STATUS, can be used to drive indication LEDs of network status. Their definitions and logic level changes upon the switch of network mode/status are described in the following tables.

Table 18: Pin Definition of Network Mode/Status Indication Pin

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	1.8 V power domain
NET_STATUS	170	DO	Indicate the module's network activity status	1.8 V power domain

Table 19: Working State of Network Mode/Status Indication Pin

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching

	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

Below is a reference design of the network indicator.

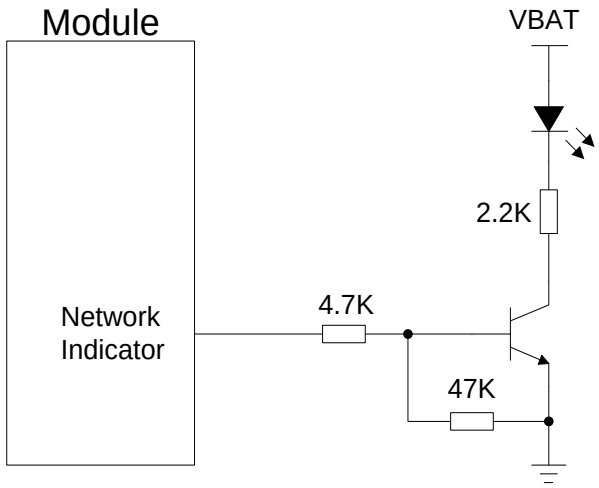


Figure 26: Reference Design of Network Indicator

3.15. STATUS

The STATUS pin is set as the module's status indicator. It outputs high level when the module is turned on.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	1.8 V power domain

The following is a reference design of the pin.

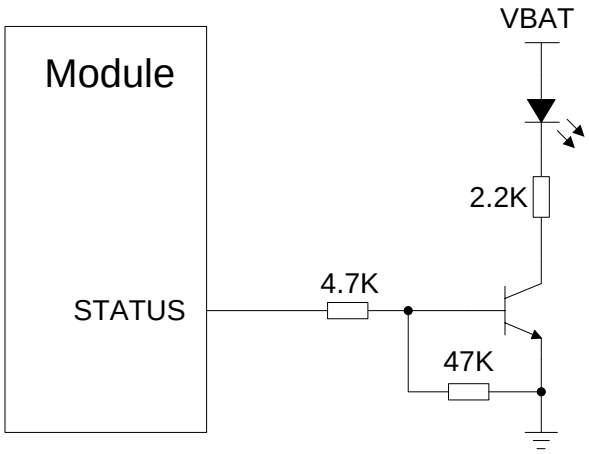


Figure 27: Reference Design of STATUS

3.16. RI Behaviors

Regardless of from which port a URC is output, it triggers the behavior of the RI pin.

NOTE

The RING URC can be output from UART port, USB AT port and USB modem port depending on the parameters of **AT+QURCCFG** command. The default port is USB AT port.

The default behavior of the RI is listed as below.

Table 21: Behavior of RI

State	Response
Idle	RI stays at high level
URC	RI outputs 100 ms low pulse when a new URC returns

3.17. PCIe Interface*

EG06 series includes a PCIe interface which is compliant with *PCI Express Base Specification Revision 2.1.* The key features of the PCIe interface are shown below:

- *PCI Express Base Specification Revision 2.1* compliance
- Data rate at 5 Gbps per lane
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 22: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)	If unused, keep it open.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)	If unused, keep it open.
PCIE_TX_M	182	AO	PCIe transmit (-)	If unused, keep it open.
PCIE_TX_P	183	AO	PCIe transmit (+)	If unused, keep it open.
PCIE_RX_M	185	AI	PCIe receive (-)	If unused, keep it open.
PCIE_RX_P	186	AI	PCIe receive (+)	If unused, keep it open.
PCIE_CLKREQ_N	188	DIO	PCIe clock request	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_RST_N	189	DIO	PCIe reset	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE_N	190	DIO	PCIe wake up	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.

In order to enhance the module's reliability and usability in applications, please follow the criteria below in PCIe interface circuit design:

- Keep PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and 19.2 MHz clock signals.
- A capacitance should be added in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length difference of Tx or Rx differential pair of PCIe routing traces less than 0.7 mm.
- Keep the differential impedance of PCIe data traces as 100 Ω ±10 %.
- Separate the SS_USB data pairs (Tx, Rx) and PCIe data pairs (Tx, Rx) from each other as far as

possible. If the SS_USB and PCIe data pairs have to cross on adjacent layers, cross them at right angles to minimize unbalanced (asymmetric) coupling.

- Do not route PCIe data traces under components or cross them with other traces.

3.17.1. Root Complex Mode

EG06 series supports Root Complex (RC) Mode through software configuration. In this mode, the module is configured to act as a PCIe RC device. The reference design of PCIe Interface in RC mode is shown as below.

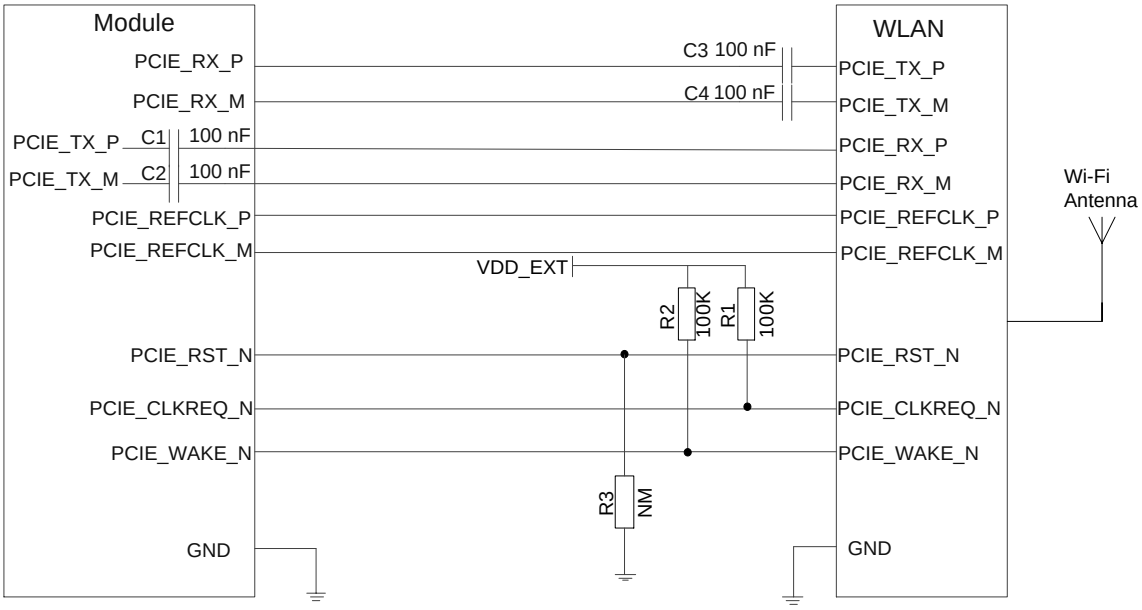


Figure 28: Reference Design of PCIe Interface (RC Mode)

3.18. WLAN Control Interface*

EG06 series provides a low-power PCIe interface* and a control interface for WLAN design. The following table shows the pin definition of WLAN control interface.

Table 23: Pin Definition of WLAN Control Interface

Pin Name	Pin No.	I/O	Description	Comment
Coexistence and Control Signal Part				
PM_ENABLE	5	DO	WLAN power supply enable control	1.8 V power domain

WAKE_ON_WIRELESS	160	DI	Wake up the host by Wi-Fi module.	1.8 V power domain
WLAN_EN	149	DO	WLAN function enable control. Active high.	1.8 V power domain
COEX_UART_RX	146	DI	LTE&WLAN coexistence signal	1.8 V power domain
COEX_UART_TX	145	DO	LTE&WLAN coexistence signal	1.8 V power domain
WLAN_SLP_CLK	169	DO	WLAN sleep clock	1.8 V power domain

3.19. SD Card Interface*

EG06 series provides one SD card interface which supports SD 3.0 protocol. The following table shows the pin definition.

Table 24: Pin Definition of the SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DATA3	48	DIO	SDIO data bit 3	If unused, keep it open.
SD_DATA2	47	DIO	SDIO data bit 2	If unused, keep it open.
SD_DATA1	50	DIO	SDIO data bit 1	If unused, keep it open.
SD_DATA0	49	DIO	SDIO data bit 0	If unused, keep it open.
SD_CLK	53	DO	SDIO clock	If unused, keep it open.
SD_CMD	51	DIO	SDIO command	If unused, keep it open.
SD_VDD	46	PO	SDIO power supply	Either 1.8 V or 3.0 V is supported by the module automatically. Power supply of SD card must be provided by an external power supply.
SD_DETECT	52	DI	SD card detect	If unused, keep it open.

The following is a reference design of the SD card interface of the module.

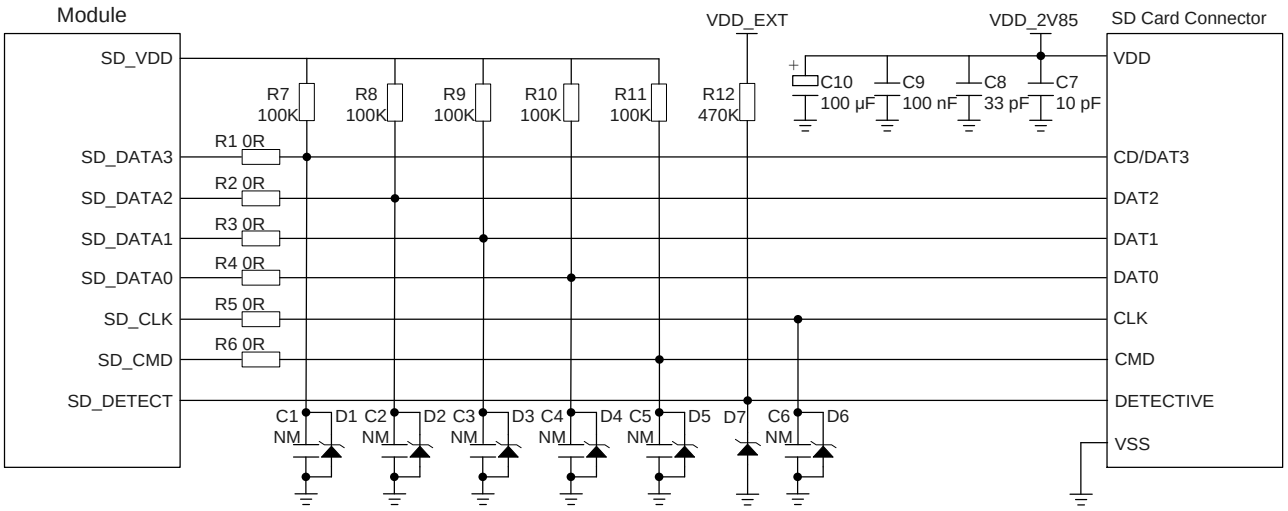


Figure 29: Reference Design of SD Card Interface

Please follow the principles below in the SD card circuit design:

- The voltage range of SD power supply VDD_2V85 is 2.7–3.6 V and a sufficient current of 0.8 A at least should be provided. As the maximum output current of VDD_SDIO is 50 mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SD_VDD. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- To offer good ESD protection, it is recommended to add a TVS diode on SD card pins.
- The load capacitance of SDIO bus needs to be less than 40 pF.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SD_CLK and SD_DATA/SD_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 36 mm, so the exterior total trace length should be less than 14 mm.
- Make sure the spacing between adjacent traces is two times the trace width and that the load capacitance of SDIO bus is less than 40 pF.

3.20. USB_BOOT Interface

EG06 series provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering on the module, and thus the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 25: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

The following is a reference design of USB_BOOT interface.

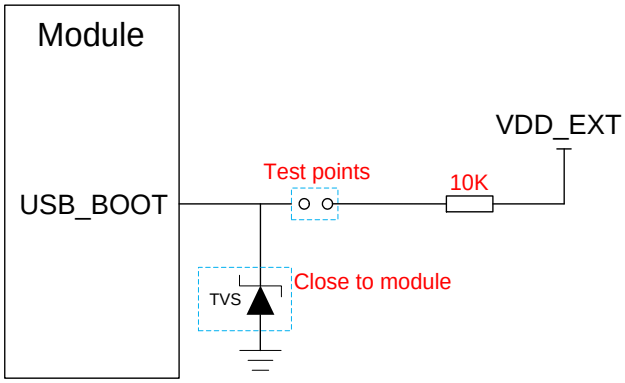


Figure 30: Reference Design of USB_BOOT Interface

3.21. SPI Interface

EG06 series provides one SPI interface multiplexed from BT UART interface. The interface only supports master mode with a maximum clock frequency up to 50 MHz.

Table 26: Pin Definition of the SPI Interface

Pin Name	Pin No.	Description	Comment
BT_TXD	163	Can be multiplexed into SPI_MOSI	1.8 V power domain.

BT_RXD	165	Can be multiplexed into SPI_MISO	If unused, keep these pins open.
BT_CTS	164	Can be multiplexed into SPI_CLK	
BT_RTS	166	Can be multiplexed into SPI_CS	

The following figure shows the timing of SPI interface. The related parameters of SPI timing are shown in the following table.

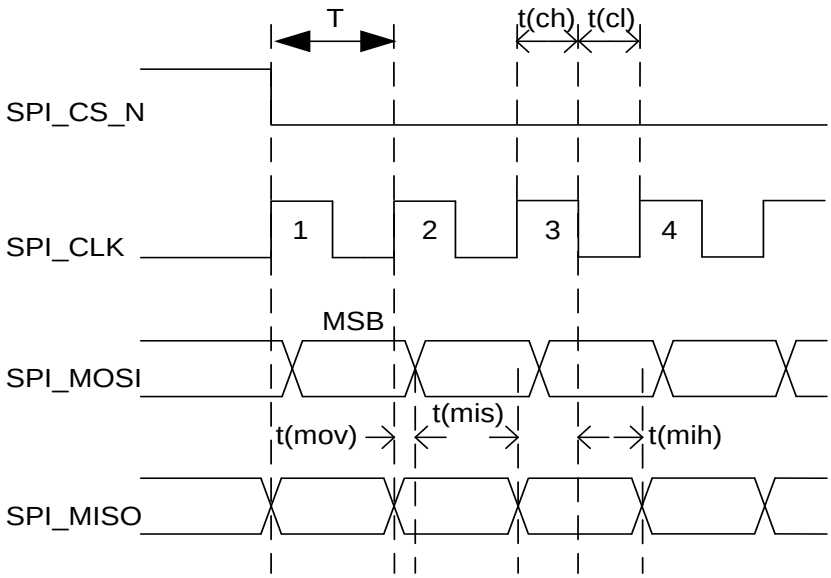


Figure 31: SPI Interface Timing

Table 27: Parameters of SPI Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

4 GNSS Receiver

4.1. General Description

EG06 series includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

The module supports standard NMEA-0183 protocol, and outputs NMEA sentence at 1 Hz data update rate via USB interface by default.

By default, the module's GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document [2]***.

4.2. GNSS Performance

Table 28: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	34.46	s
		XTRA enabled	11.19	s
	Warm start @ open sky	Autonomous	27.37	s
		XTRA enabled	2.06	s
	Hot start @ open sky	Autonomous	2.36	s
		XTRA enabled	1.63	s

Accuracy (GNSS)	CEP-50	Autonomous @ open sky	2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port for the module to keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port for the module to fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port for the module to fix position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be followed in your design.

- Maximize the distance among GNSS antenna, Main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance of ANT_GNSS trace at 50 Ω.

See ***Chapter 5*** for GNSS reference design and antenna installation information.

5 Antenna Interfaces

EG06 series includes a Main antenna interface, a Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main/Rx-diversity Antenna Interface

5.1.1. Pin Definition

Table 29: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	107	DIO	Main antenna interface	50 Ω impedance
ANT_DIV	127	AI	Receive diversity antenna interface	50 Ω impedance. If unused, keep it open.

5.1.2. Operating Frequency

Table 30: EG06-E Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE B1	1920–1980	2110–2170	MHz
LTE B3	1710–1785	1805–1880	MHz
LTE B5	824–849	869–894	MHz

LTE B7	2500–2570	2620–2690	MHz
LTE B8	880–915	925–960	MHz
LTE B20	832–862	791–821	MHz
LTE B28	703–748	758–803	MHz
LTE B32	-	1452–1496	MHz
LTE B38	2570–2620	2570–2620	MHz
LTE B40	2300–2400	2300–2400	MHz
LTE B41	2545–2655	2545–2655	MHz

Table 31: EG06-A Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
LTE B2	1850–1910	1930–1990	MHz
LTE B4	1710–1755	2110–2155	MHz
LTE B5	824–849	869–894	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B12	699–716	729–746	MHz
LTE B13	777–787	746–756	MHz
LTE B25	1850–1915	1930–1995	MHz
LTE B26	814–849	859–894	MHz
LTE B29	-	717–728	MHz
LTE B30	2305–2315	2350–2360	MHz
LTE B66	1710–1780	2110–2200	MHz

Table 32: EG06-AUTL Operating Frequencies

3GPP Band	Transmit	Receive	Unit
LTE B3	1710–1785	1805–1880	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B28	703–748	758–803	MHz

Table 33: EG06-EA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE B1	1920–1980	2110–2170	MHz
LTE B3	1710–1785	1805–1880	MHz
LTE B5	824–849	869–894	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B8	880–915	925–960	MHz
LTE B20	832–862	791–821	MHz
LTE B28	703–748	758–803	MHz
LTE B32	-	1452–1496	MHz
LTE B38	2570–2620	2570–2620	MHz
LTE B40	2300–2400	2300–2400	MHz
LTE B41	2496–2690	2496–2690	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna interfaces is shown as below. The π-type matching circuits should be reserved for better RF performance. The capacitors are not mounted by default.

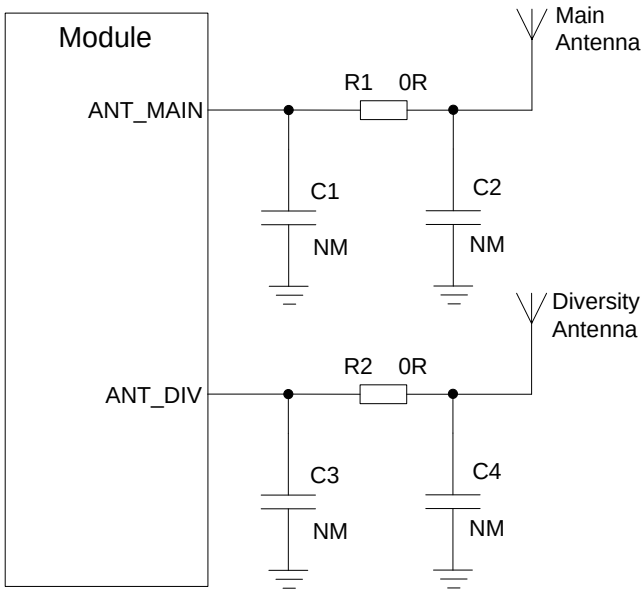


Figure 32: Reference Design of RF Antenna Interface

NOTES

1. Keep a proper distance between the Main and Rx-diversity antennas to improve receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity.
3. Place the π-type matching components (R1/C1/C2 and R2/C3/C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For the module to be applicable to your PCB, the characteristic impedance of all RF traces should be controlled at 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

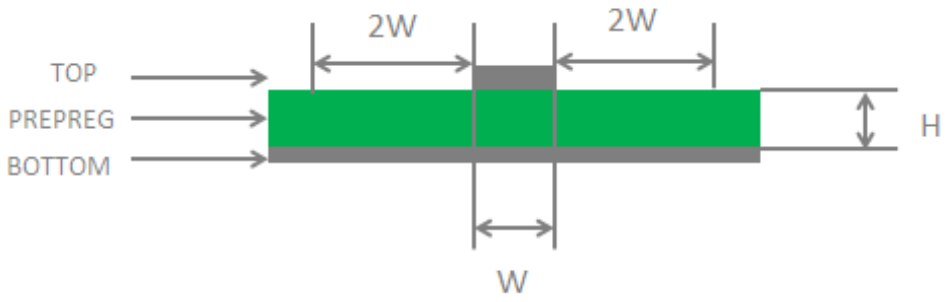


Figure 33: Reference Design of Microstrip on 2-layer PCB

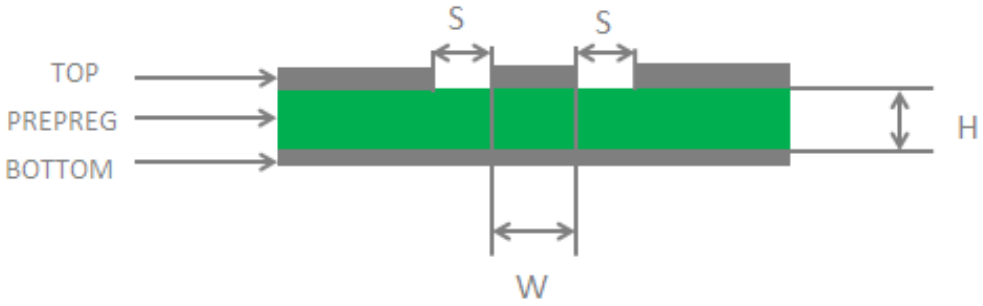


Figure 34: Reference Design of Coplanar Waveguide on 2-layer PCB

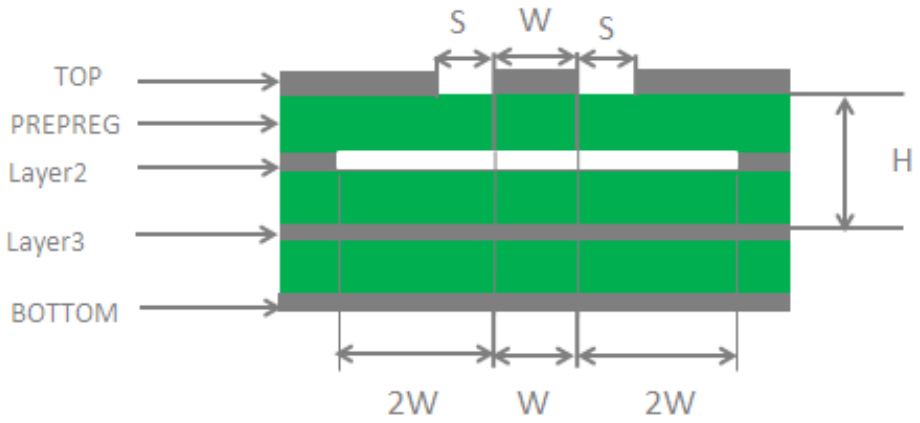


Figure 35: Reference Design of Coplanar Waveguide on 4-layer PCB (Layer 3 as Ref. Ground)

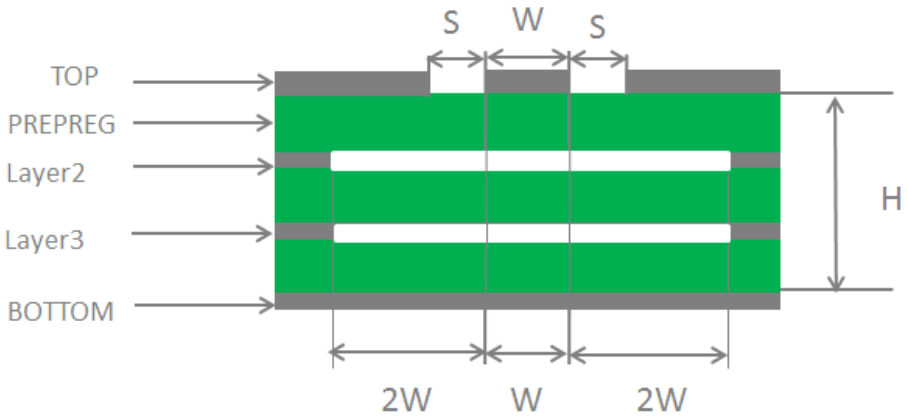


Figure 36: Reference Design of Coplanar Waveguide on 4-layer PCB (Layer 4 as Ref. Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces at 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground can help improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).

For more details about RF layout, see ***document [5]***.

5.2. GNSS Antenna Interface

Table 34: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50 Ω impedance

Table 35: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

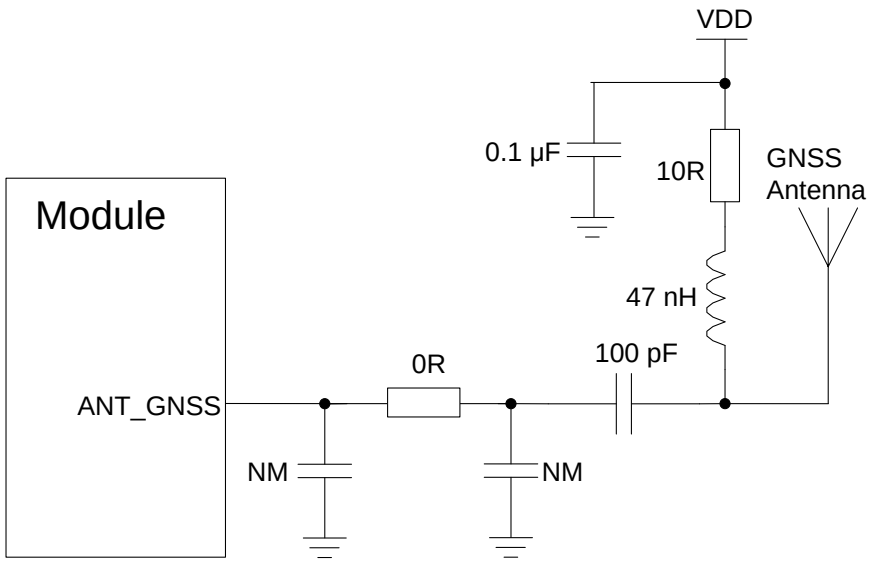


Figure 37: Reference Design of GNSS Antenna

NOTES

1. According to the active antenna requirement, an external LDO can be applied while supplying power to the module.
2. If the module is designed with a passive antenna, the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on Main antenna, Rx-diversity antenna and GNSS antenna.

Table 36: Antenna Requirements

Type	Requirements
GNSS [1)]	Frequency Range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi Active Antenna Noise Figure: < 1.5 dB Active Antenna Gain: > 0 dBi Active Antenna Embedded LNA Gain: < 17 dB
WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (WCDMA B5/B8, LTE B5/B8/B12/B13/B20/B26/B28/B29) Cable Insertion Loss: < 1.5 dB (WCDMA B1/B2/B3/B4, LTE B1/B2/B3/B4/B25/B32/B39/B66) Cable Insertion Loss < 2 dB (LTE B7/B38/B40/B41/B30)

NOTE

As the harmonics generated by LTE B13 and B14 may saturate the LNA of active antennas, it is recommended to use the passive antenna in such networks.

5.3.2. Recommended RF Connector for Antenna Installation

If an RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *Hirose*.

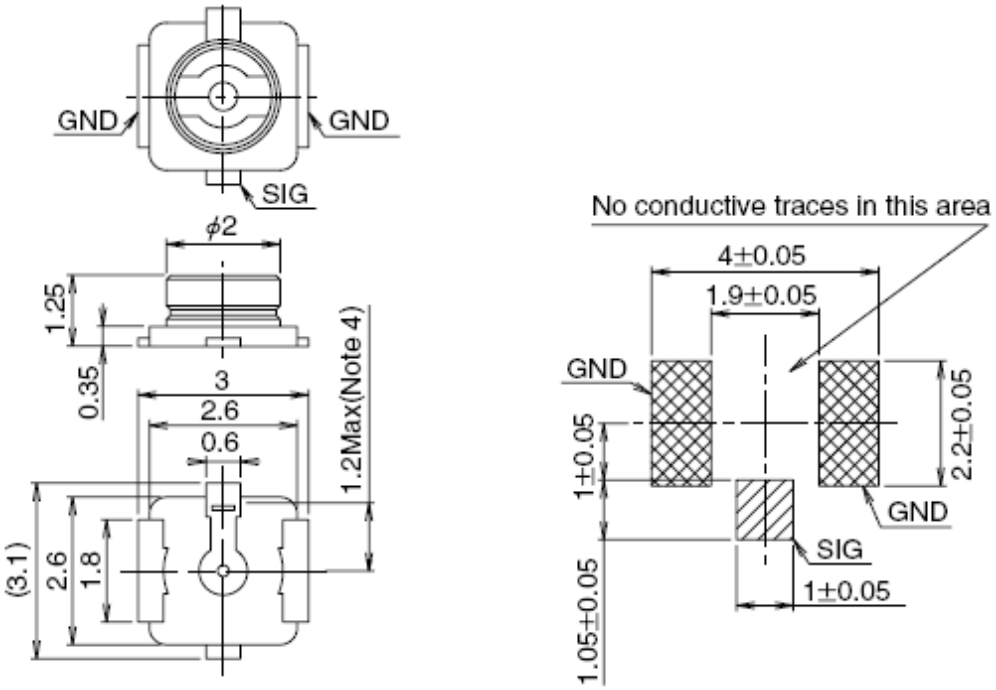


Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP connector series listed in the following figure can be used to match the U.FL-R-SMT.

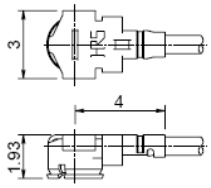
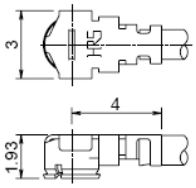
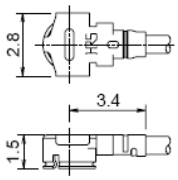
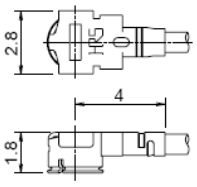
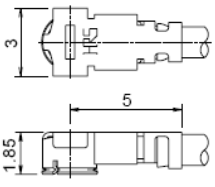
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Mechanical Features of U.FL-LP Connectors

The following figure illustrates the space factor of mated connectors.

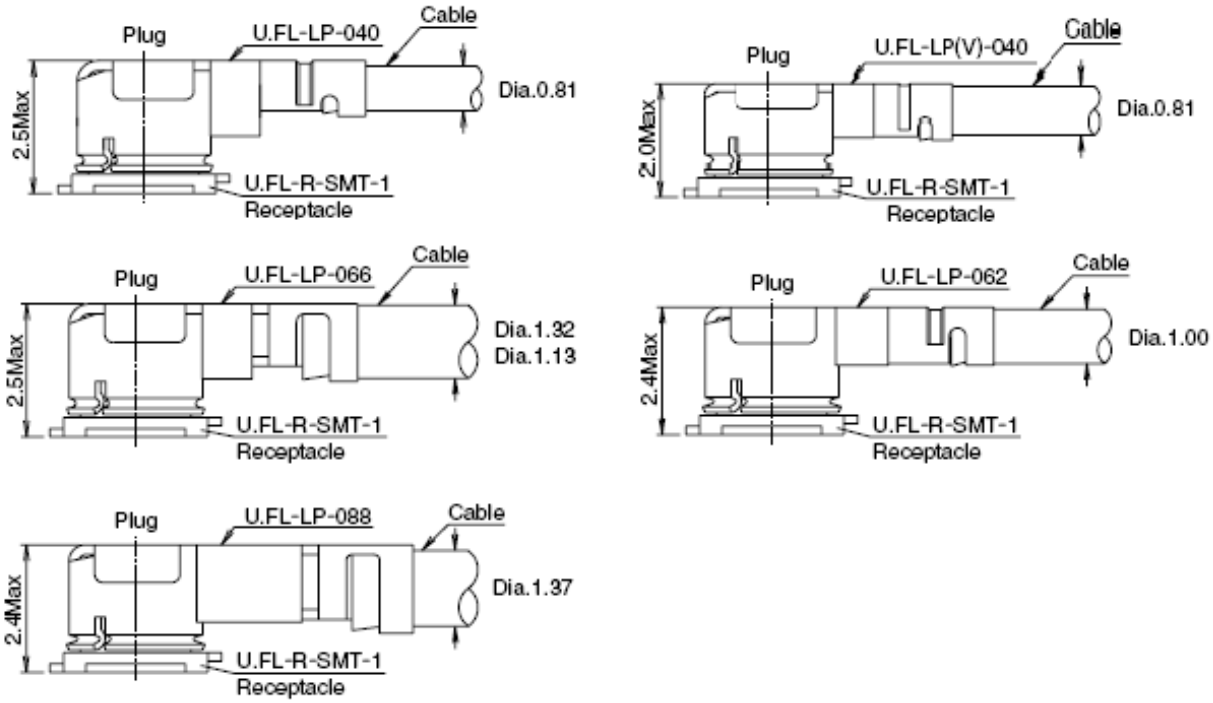


Figure 40: Space Factor of Mated Connectors (Unit: mm)

For more details, visit https://www.hirose.com.

6 Reliability, Radio and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.2	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 38: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Operating and Storage Temperatures

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module keeps the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There won't be unrecoverable malfunctions. Nor will there be effects on the radio spectrum or harm to radio networks. Only one or more parameters like P_{out} might reduce in the value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

Table 40: EG06-E Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	10	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.12	mA
	WCDMA PF = 64 (USB disconnected)	1.53	mA
	WCDMA PF = 128 (USB disconnected)	1.52	mA
	WCDMA PF = 512 (USB disconnected)	1.54	mA
	LTE-FDD PF = 32 (USB disconnected)	2.68	mA
	LTE-FDD PF = 64 (USB disconnected)	2.67	mA
	LTE-FDD PF = 128 (USB disconnected)	2.68	mA
	LTE-TDD PF = 32 (USB disconnected)	2.7	mA
	LTE-TDD PF = 64 (USB disconnected)	2.69	mA
	LTE-TDD PF = 128 (USB disconnected)	2.69	mA
Idle state	WCDMA PF = 64 (USB disconnected)	18	mA
	WCDMA PF = 64 (USB connected)	27.2	mA
	LTE-FDD PF = 64 (USB disconnected)	22.3	mA
	LTE-FDD PF = 64 (USB connected)	28.4	mA
	LTE-TDD PF = 64 (USB disconnected)	21.8	mA
	LTE-TDD PF = 64 (USB connected)	28	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 22.7 dBm	445	mA
	WCDMA B1 HSUPA CH10700 @ 22.2 dBm	450	mA
	WCDMA B3 HSDPA CH1338 @ 22.8 dBm	627	mA
	WCDMA B3 HSUPA CH1338 @ 22.3 dBm	635	mA

	WCDMA B5 HSDPA CH4407 @ 22.7 dBm	540	mA
	WCDMA B5 HSUPA CH4407 @ 22.3 dBm	549	mA
	WCDMA B8 HSDPA CH3012 @ 22.6 dBm	550	mA
	WCDMA B8 HSUPA CH3012 @ 22.4 dBm	560	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH300 @ 23.5 dBm	587	mA
	LTE-FDD B3 CH1575 @ 23.7 dBm	790	mA
	LTE-FDD B5 CH2525 @ 22.7 dBm	532	mA
	LTE-FDD B7 CH3100 @ 23.48 dBm	803.2	mA
	LTE-FDD B8 CH3625 @ 23.83 dBm	616.9	mA
	LTE-FDD B20 CH6300 @ 23.05 dBm	639.5	mA
	LTE-FDD B28 CH27460 @ 23.01 dBm	711	mA
	LTE-TDD B38 CH38000 @ 23.88 dBm	383.4	mA
	LTE-TDD B40 CH39150 @ 23.67 dBm	341.3	mA
	LTE-TDD B41 CH40740 @ 23.88 dBm	375.3	mA
2CA data transfer	LTE-FDD B1 + B1 @ 21.05 dBm	618.7	mA
	LTE-FDD B1 + B5 @ 21.07 dBm	769.9	mA
	LTE-FDD B1 + B8 @ 21.91 dBm	619.1	mA
	LTE-FDD B1 + B20 @ 20.91 dBm	633	mA
	LTE-FDD B1 + B28 @ 21.09 dBm	746.8	mA
	LTE-FDD B3 + B3 @ 21.74 dBm	740.5	mA
	LTE-FDD B3 + B5 @ 21.18 dBm	751	mA
	LTE-FDD B3 + B7 @ 21.1 dBm	789.1	mA
	LTE-FDD B3 + B8 @ 21.2 dBm	748.2	mA
	LTE-FDD B3 + B20 @ 21.16 dBm	779.3	mA
	LTE-FDD B3 + B28 @ 21.12 dBm	786.7	mA

	LTE-FDD B7 + B5 @ 21.29 dBm	848.3	mA
	LTE-FDD B7 + B7 @ 21.33 dBm	834.9	mA
	LTE-FDD B7 + B8 @ 21.3 dBm	852.3	mA
	LTE-FDD B7 + B20 @ 21.32 dBm	885.9	mA
	LTE-FDD B7 + B28 @ 21.33 dBm	881.7	mA
	LTE-FDD B20 + B32 @ 20.88 dBm	693	mA
	LTE-TDD B38 + B38 @ 21.3 dBm	400.5	mA
	LTE-TDD B40 + B40 @ 20.99 dBm	369.3	mA
	LTE-TDD B41 + B41 @ 21.25 dBm	403.9	mA
WCDMA voice call	WCDMA B1 CH10700 @ 2283 dBm	450.3	mA
	WCDMA B3 CH1338 @ 22.97 dBm	650.3	mA
	WCDMA B5 CH4407 @ 22.75 dBm	556.3	mA
	WCDMA B8 CH3012 @ 22.89 dBm	568	mA

Table 41: EG06-A Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	8	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.12	mA
	WCDMA PF = 64 (USB disconnected)	2.12	mA
	WCDMA PF = 128 (USB disconnected)	1.77	mA
	WCDMA PF = 512 (USB disconnected)	1.46	mA
	LTE-FDD PF = 32 (USB disconnected)	3.92	mA
	LTE-FDD PF = 64 (USB disconnected)	2.72	mA
	LTE-FDD PF = 128 (USB disconnected)	2.10	mA
Idle state	WCDMA PF = 64 (USB disconnected)	20.31	mA

	WCDMA PF = 64 (USB connected)	21.06	mA
	LTE-FDD PF = 64 (USB disconnected)	20.94	mA
	LTE-FDD PF = 64 (USB connected)	21.53	mA
WCDMA data transfer (GNSS OFF)	WCDMA B2 HSDPA CH9800 @ 22.58 dBm	539.16	mA
	WCDMA B2 HSUPA CH9800 @ 22.56 dBm	568.51	mA
	WCDMA B4 HSDPA CH1638 @ 22.49 dBm	593.97	mA
	WCDMA B4 HSUPA CH1638 @ 22.51 dBm	675.57	mA
	WCDMA B5 HSDPA CH4407 @ 22.35 dBm	527.49	mA
	WCDMA B5 HSUPA CH4407 @ 22.32 dBm	542.53	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH900 @ 23.26 dBm	682.37	mA
	LTE-FDD B4 CH2175 @ 23.14 dBm	775.8	mA
	LTE-FDD B5 CH2525 @ 23.2 dBm	604.34	mA
	LTE-FDD B7 CH3100 @ 23.21 dBm	862.19	mA
	LTE-FDD B12 CH5095 @ 23.12 dBm	600.83	mA
	LTE-FDD B13 CH5230 @ 23.24 dBm	614.1	mA
	LTE-FDD B25 CH8365 @ 23.32 dBm	642.87	mA
	LTE-FDD B26 CH8865 @ 23.47 dBm	652.75	mA
	LTE-FDD B30 CH9820 @ 23.32 dBm	724.75	mA
	LTE-FDD B66 CH132322 @ 23.23 dBm	741.32	mA
2CA data transfer	LTE-FDD B2 + B2 @ 23.34 dBm	781.47	mA
	LTE-FDD B2 + B5 @ 23.39 dBm	721.55	mA
	LTE-FDD B2 + B12 @ 23.38 dBm	724.87	mA
	LTE-FDD B2 + B13 @ 23.38 dBm	726.42	mA
	LTE-FDD B2 + B29 @ 23.39 dBm	733.88	mA
	LTE-FDD B4 + B4 @ 23.07 dBm	749.39	mA

	LTE-FDD B4 + B5 @ 23.15 dBm	773.46	mA
	LTE-FDD B4 + B12 @ 23.17 dBm	785.31	mA
	LTE-FDD B4 + B13 @ 23.16 dBm	788.06	mA
	LTE-FDD B4 + B29 @ 23.18 dBm	793.44	mA
	LTE-FDD B5 + B7 @ 23.2 dBm	701.07	mA
	LTE-FDD B5 + B25 @ 23.23 dBm	698.8	mA
	LTE-FDD B5 + B30 @ 23.22 dBm	686.67	mA
	LTE-FDD B5 + B66 @ 23.21 dBm	724.38	mA
	LTE-FDD B12 + B7 @ 23.09 dBm	733.25	mA
	LTE-FDD B12 + B25 @ 23.1 dBm	739.42	mA
	LTE-FDD B12 + B30 @ 23.12 dBm	702.48	mA
	LTE-FDD B12 + B66 @ 23.08 dBm	729.29	mA
	LTE-FDD B13 + B66 @ 23.16 dBm	752.33	mA
	LTE-FDD B25 + B25 @ 23.21 dBm	816.88	mA
	LTE-FDD B25 + B26 @ 23.28 dBm	763.82	mA
	LTE-FDD B26 + B7 @ 23.34 dBm	742.52	mA
	LTE-FDD B30 + B29 @ 23.04 dBm	798.66	mA
	LTE-FDD B66 + B29 @ 23.31 dBm	797.14	mA
	LTE-FDD B66 + B66 @ 23.24 dBm	847.55	mA
WCDMA voice call	WCDMA B2 CH9800 @ 23.14 dBm	556.44	mA
	WCDMA B4 CH1638 @ 23.1 dBm	669.15	mA
	WCDMA B5 CH4407 @ 23.33 dBm	562.6	mA

Table 42: EG06-EA Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.25	mA
	WCDMA PF = 64 (USB disconnected)	2.31	mA
	WCDMA PF = 128 (USB disconnected)	1.92	mA
	WCDMA PF = 512 (USB disconnected)	1.64	mA
	LTE-FDD PF = 32 (USB disconnected)	4.05	mA
	LTE-FDD PF = 64 (USB disconnected)	2.90	mA
	LTE-FDD PF = 128 (USB disconnected)	2.29	mA
	LTE-TDD PF = 32 (USB disconnected)	4.26	mA
	LTE-TDD PF = 64 (USB disconnected)	2.98	mA
	LTE-TDD PF = 128 (USB disconnected)	2.33	mA
Idle state	WCDMA PF = 64 (USB disconnected)	20.10	mA
	WCDMA PF = 64 (USB connected)	29.12	mA
	LTE-FDD PF = 64 (USB disconnected)	20.81	mA
	LTE-FDD PF = 64 (USB connected)	29.52	mA
	LTE-TDD PF = 64 (USB disconnected)	20.07	mA
	LTE-TDD PF = 64 (USB connected)	29.68	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 22.24dBm	532.55	mA
	WCDMA B1 HSUPA CH10700 @ 22.31 dBm	560.82	mA
	WCDMA B3 HSDPA CH1338 @ 22.20 dBm	509.88	mA
	WCDMA B3 HSUPA CH1338 @ 22.31 dBm	489.66	mA
	WCDMA B5 HSDPA CH4407 @ 22.17dBm	500.22	mA
	WCDMA B5 HSUPA CH4407 @ 22.36 dBm	533.74	mA

	WCDMA B8 HSDPA CH3012 @ 22.29dBm	532.70	mA
	WCDMA B8 HSUPA CH3012 @ 22.45 dBm	544.89	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH300 @ 23.20 dBm	676.59	mA
	LTE-FDD B3 CH1575 @ 23.34 dBm	599.62	mA
	LTE-FDD B5 CH2525 @ 23.48 dBm	601.32	mA
	LTE-FDD B7 CH3100 @ 23.13 dBm	787.64	mA
	LTE-FDD B8 CH3625 @ 23.49 dBm	652.43	mA
	LTE-FDD B20 CH6300 @ 23.49 dBm	719.22	mA
	LTE-FDD B28A CH9360 @ 23.08 dBm	717.91	mA
	LTE-FDD B28B CH9510 @ 23.27 dBm	667.79	mA
	LTE-TDD B38 CH38000 @ 23.19 dBm	426.44	mA
	LTE-TDD B40 CH39150 @ 23.42 dBm	350.88	mA
	LTE-TDD B41 CH40740 @ 22.80 dBm	422.79	mA
2CA data transfer	LTE-FDD B1 + B1 @ 23.13 dBm	817.91	mA
	LTE-FDD B1 + B3 @ 23.18 dBm	785.1	mA
	LTE-FDD B1 + B5 @ 23.13 dBm	758.08	mA
	LTE-FDD B1 + B7 @ 23.10 dBm	793.14	mA
	LTE-FDD B1 + B8 @ 23.07 dBm	760.47	mA
	LTE-FDD B1 + B20 @ 23.18 dBm	790.15	mA
	LTE-FDD B1 + B28 @ 23.18 dBm	791.33	mA
	LTE-FDD B3 + B3 @ 23.18 dBm	712.31	mA
	LTE-FDD B3 + B5 @ 23.23 dBm	672.03	mA
	LTE-FDD B3 + B7 @ 23.13 dBm	704.51	mA
	LTE-FDD B3 + B8 @ 23.30 dBm	673.94	mA
	LTE-FDD B3 + B20 @ 23.14 dBm	703.24	mA

	LTE-FDD B3 + B28 @ 23.30 dBm	705.02	mA
	LTE-FDD B5 + B5 @ 23.32 dBm	677.38	mA
	LTE-FDD B5 + B7 @ 23.46 dBm	695.07	mA
	LTE-FDD B7 + B7 @ 23.06 dBm	961.26	mA
	LTE-FDD B7 + B8 @ 22.90 dBm	848.5	mA
	LTE-FDD B7 + B20 @ 22.86 dBm	879.92	mA
	LTE-FDD B7 + B28 @ 23.39 dBm	882.6	mA
	LTE-FDD B20 + B32 @ 23.36 dBm	890.6	mA
	LTE-TDD B38 + B38 @ 23.38 dBm	460.78	mA
	LTE-TDD B40 + B40 @ 23.28 dBm	406.53	mA
	LTE-TDD B41 + B41 @ 23.27 dBm	524.02	mA
WCDMA voice call	WCDMA B1 CH10700 @ 23.25 dBm	577.37	mA
	WCDMA B3 CH1338 @ 23.27 dBm	548.77	mA
	WCDMA B5 CH4407 @ 23.20 dBm	546.55	mA
	WCDMA B8 CH3012 @ 23.28 dBm	579.47	mA

6.5. RF Output Power

The following table shows the RF output power of the module.

Table 43: RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
WCDMA bands	24 dBm +1/-3 dB	< -50 dBm
LTE FDD bands	23 dBm ±2 dB	< -40 dBm
LTE TDD bands	23 dBm ±2 dB	< -40 dBm

6.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of the module.

Table 44: EG06-E Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA B1	-108.5 dBm	-109.5 dBm	-	-106.7 dBm
WCDMA B3	-109.0 dBm	-107.0 dBm	-	-103.7 dBm
WCDMA B5	-108.5 dBm	-109.5 dBm	-	-104.7 dBm
WCDMA B8	-110.0 dBm	-109.5 dBm	-	-103.7 dBm
LTE-FDD B1 (10 MHz)	-97.0 dBm	-98.0 dBm	-101.0 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-97.5 dBm	-96.5 dBm	-100.0 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-96.0 dBm	-98.5 dBm	-100.5 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.0 dBm	-96.5 dBm	-99.5 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.0 dBm	-98.5 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-97.0 dBm	-99.0 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.0 dBm	-97.5 dBm	-101.0 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-96.5 dBm	-96.0 dBm	-99.0 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.0 dBm	-97.0 dBm	-100.5 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-96.0 dBm	-96.0 dBm	-99.0 dBm	-94.3 dBm

Table 45: EG06-A Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA B2	-109 dBm	-109 dBm	-	-104.7 dBm
WCDMA B4	-109 dBm	-110 dBm	-	-106.7 dBm
WCDMA B5	-110 dBm	-110 dBm	-	-104.7 dBm

LTE-FDD B2 (10 MHz)	-97.4 dBm	-97.4 dBm	-100.1 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.1 dBm	-97.8 dBm	-100 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.3 dBm	-99.3 dBm	-102 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.6 dBm	-97 dBm	-99.3 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99 dBm	-99.3 dBm	-102 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98.8 dBm	-99.5 dBm	-101.8 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97 dBm	-97.3 dBm	-100.1 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.2 dBm	-99.8 dBm	-102.1 dBm	-93.8 dBm
LTE-FDD B30 (10 MHz)	-97 dBm	-97.5 dBm	-99.9 dBm	-95.3 dBm
LTE-FDD B66 (10 MHz)	-96.3 dBm	-97.8 dBm	-99.7 dBm	-95.8 dBm

Table 46: EG06-EA Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA B1	-110 dBm	-110 dBm	-	-106.7 dBm
WCDMA B3	-110.5 dBm	-110.5 dBm	-	-103.7 dBm
WCDMA B5	-110.5 dBm	-112 dBm	-	-104.7 dBm
WCDMA B8	-111 dBm	-111.5 dBm	-	-104.7 dBm
LTE-FDD B1 (10 MHz)	-97.7 dBm	-98.4 dBm	-100.6 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.0 dBm	-98.3 dBm	-101.4 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-98.1 dBm	-100.1 dBm	-101.9 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.7 dBm	-98.0 dBm	-100.0 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.6 dBm	-99.0 dBm	-101.6 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98.2 dBm	-100.4 dBm	-102.3 dBm	-93.3 dBm
LTE-FDD B28A (10 MHz)	-99.4 dBm	-100.9 dBm	-103.0 dBm	-94.8 dBm
LTE-FDD B28B (10 MHz)	-99.8 dBm	-100.6 dBm	-103.2 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-97.6 dBm	-97.9 dBm	-99.7 dBm	-96.3 dBm

LTE-TDD B40 (10 MHz)	-97.7 dBm	-98.6 dBm	-100.4 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.2 dBm	-97.1 dBm	-99.4 dBm	-94.3 dBm

NOTE

1) SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side to improve Rx performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of the module.

Table 47: Electrostatic Discharge Characteristics

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

To achieve better performance of the module, it is recommended to comply with the following principles out of thermal considerations:

- In your PCB design, place the module away from heating sources, especially high power components, such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted and do not fill that area with copper, allowing for the adding of heatsink when necessary.
- Ensure the reference ground of the area where the module is mounted is complete, and add as many

ground vias as possible for better heat dissipation.

- Make sure the ground pads of the module and PCB are fully connected.
- According to particular application demands, mount the heatsink on the top of the module, or the opposite side of the PCB area where the module is mounted, or on both.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between heatsink and module/PCB.

Below are two reference designs of the heatsink. You can choose one or both of them according to application structures.

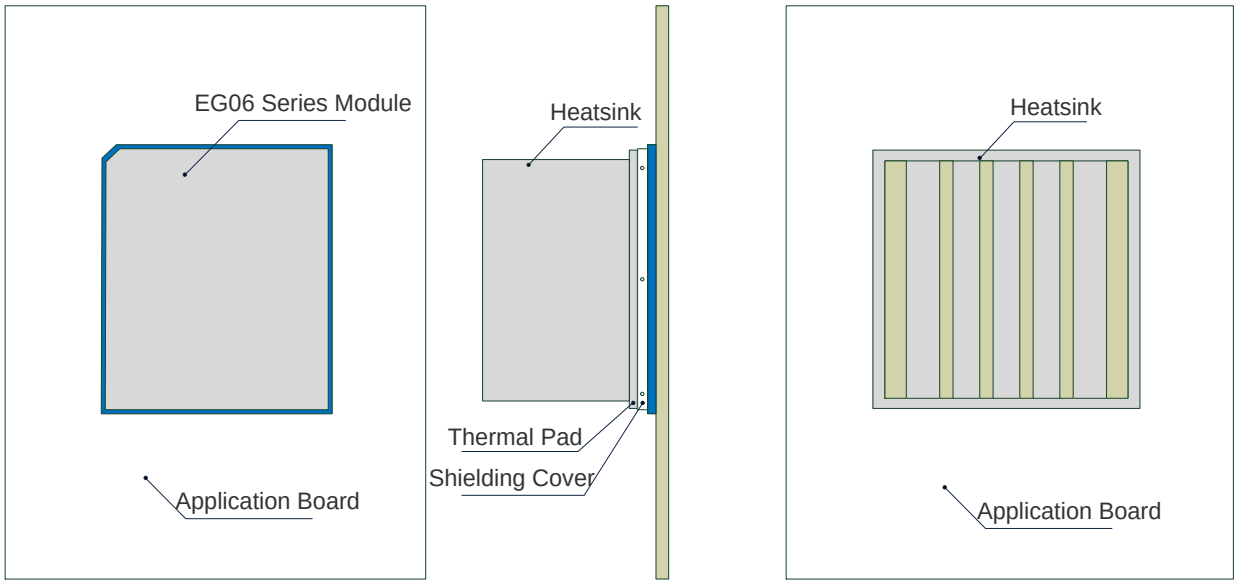


Figure 41: Reference Design of Heatsink (Heatsink at the Top of the Module)

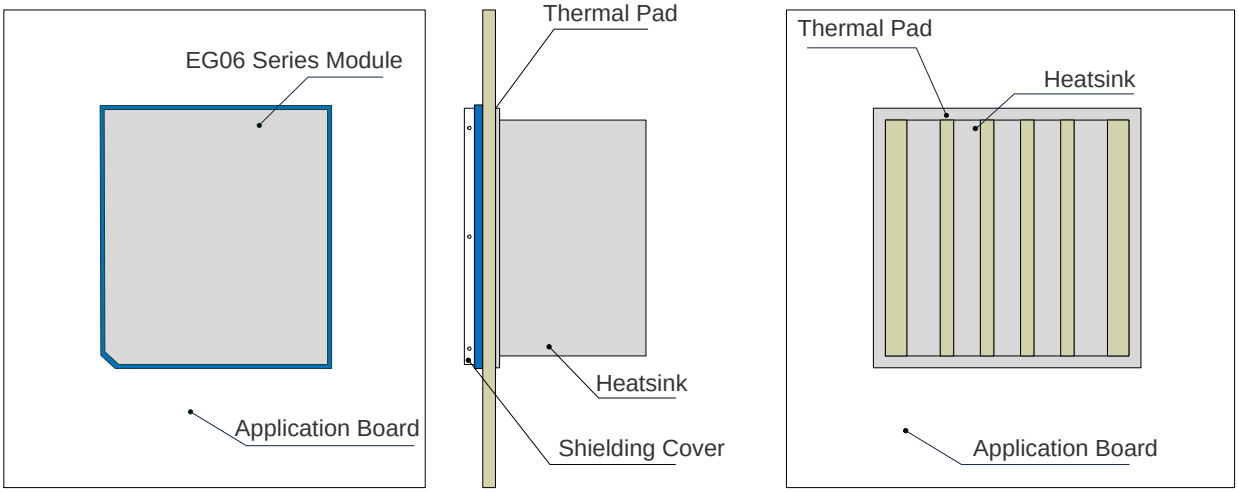


Figure 42: Reference Design of Heatsink (Heatsink at the Backside of PCB)

NOTES

1. Make sure that your PCB design provides sufficient cooling for the module: proper mounting, heatsinks, and active cooling may be required depending on the integrated application.
2. To protect components from damage, the thermal design should be optimized to the largest possible extent to maintain the module's internal temperature below 105 °C. You can execute **AT+QTEMP** command to get the module's internal temperature.
3. For more detailed guidelines on thermal design, see ***document [6]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

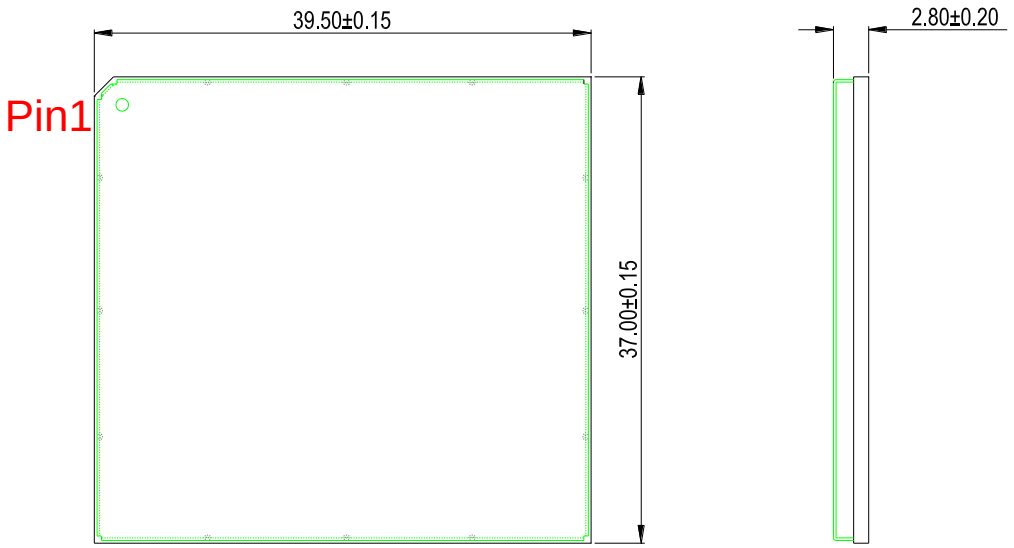


Figure 43: Top and Side Dimensions

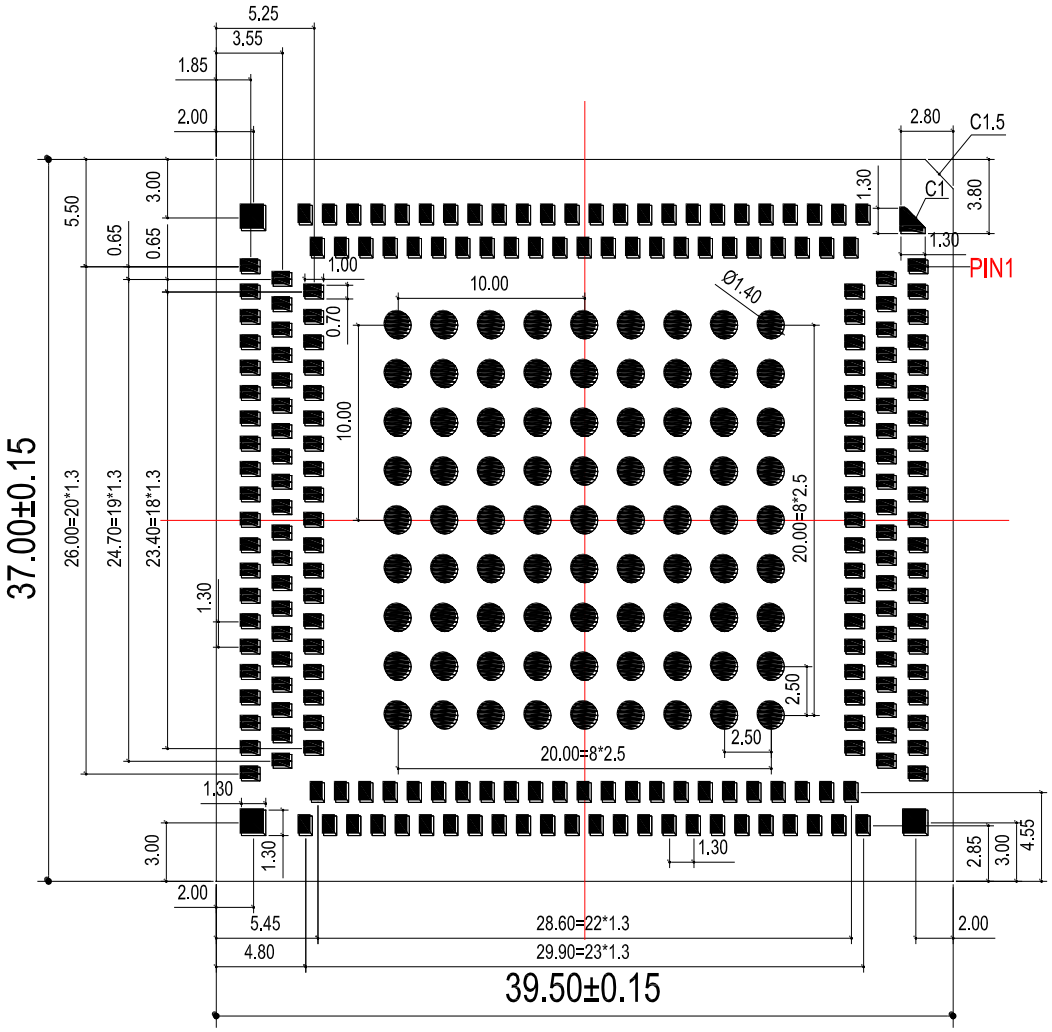


Figure 44: Bottom Dimensions

7.2. Recommended Footprint

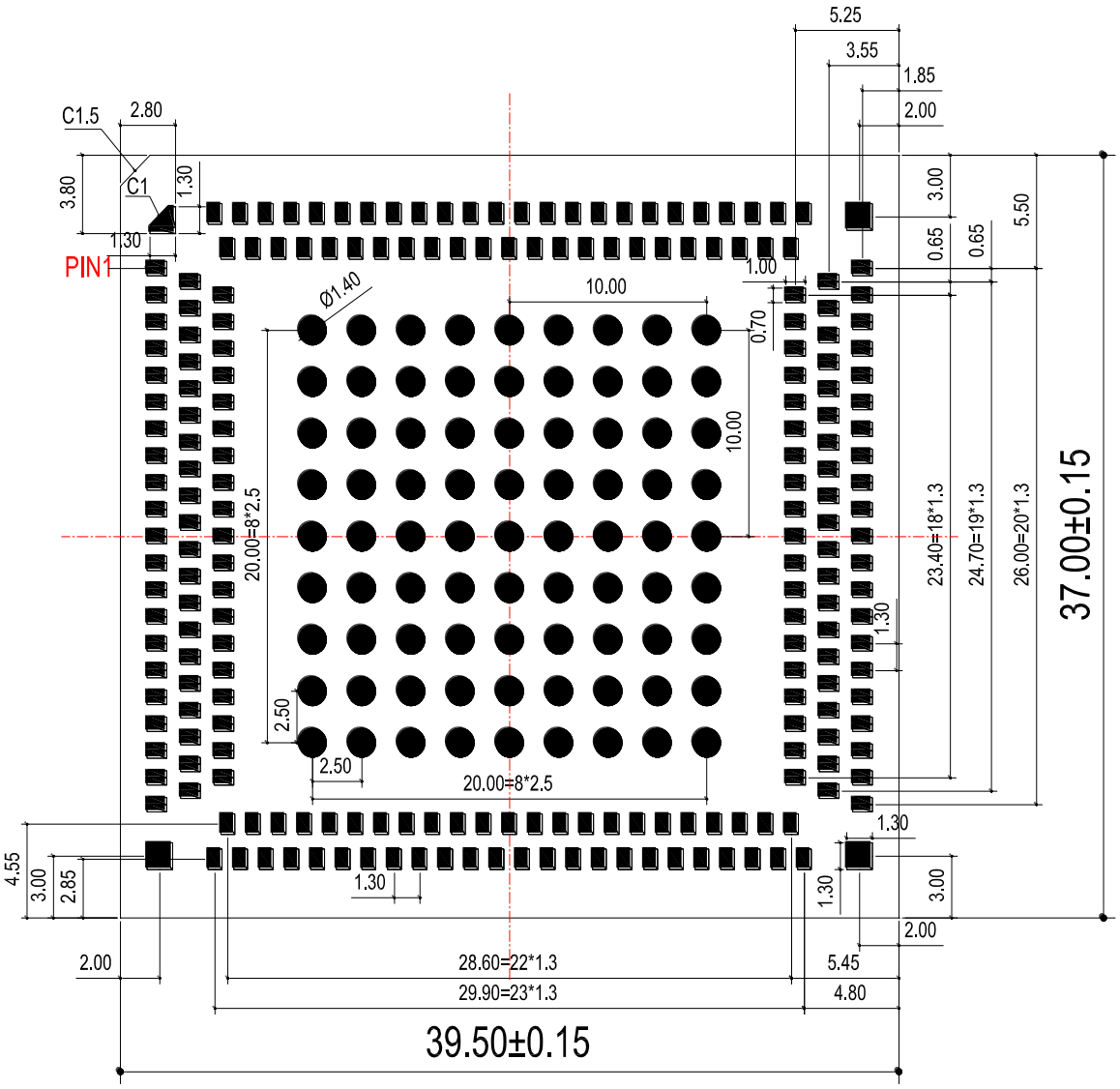


Figure 45: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the host PCB.
2. The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.3. Drawings of the Module

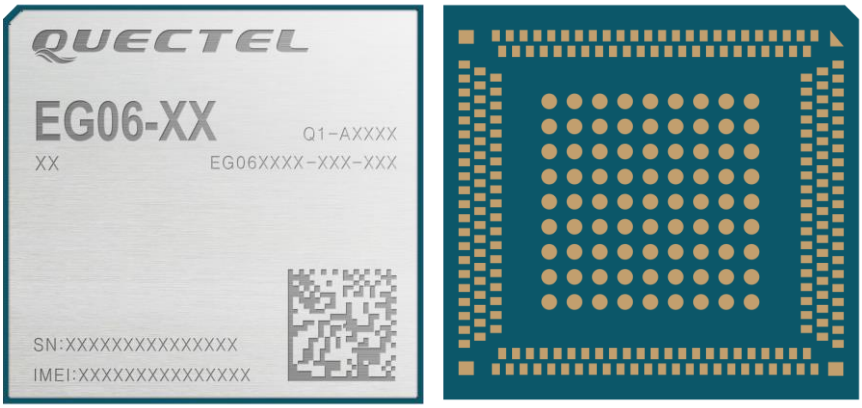


Figure 46: Top & Bottom Views

NOTES

1. Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. The package warpage level of the module conforms to *JEITA ED-7306* standard.

8 Storage, Manufacturing and Packaging

8.1. Storage

EG06 series is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, It is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module should be 0.13–0.15 mm. For more details, see ***document [3]***.

It is suggested that the peak reflow temperature is 238–246 ºC and the absolute max reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

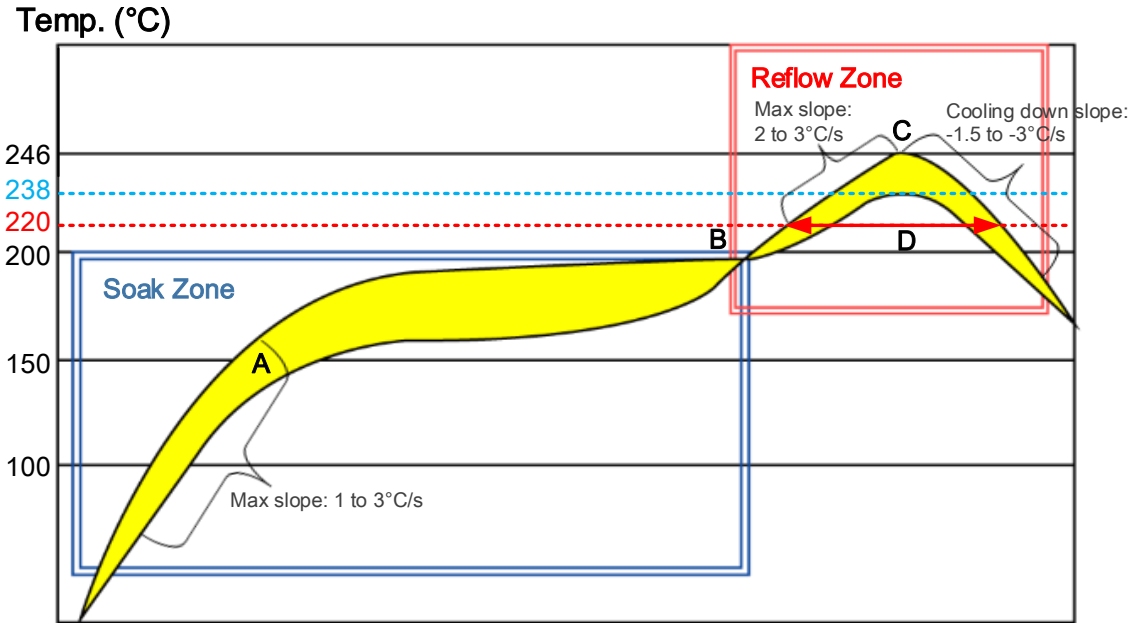


Figure 47: Recommended Reflow Soldering Thermal Profile

Table 48: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 s
Reflow Zone	
Max slope	2–3°C/s
Reflow time (D: over 220 °C)	40–70 s
Max temperature	238–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

8.3. Packaging

EG06 series is packaged in tape and reel carriers. One reel is 10.56 meters long and contains 200 modules. The figures below show the packaging details, measured in mm.

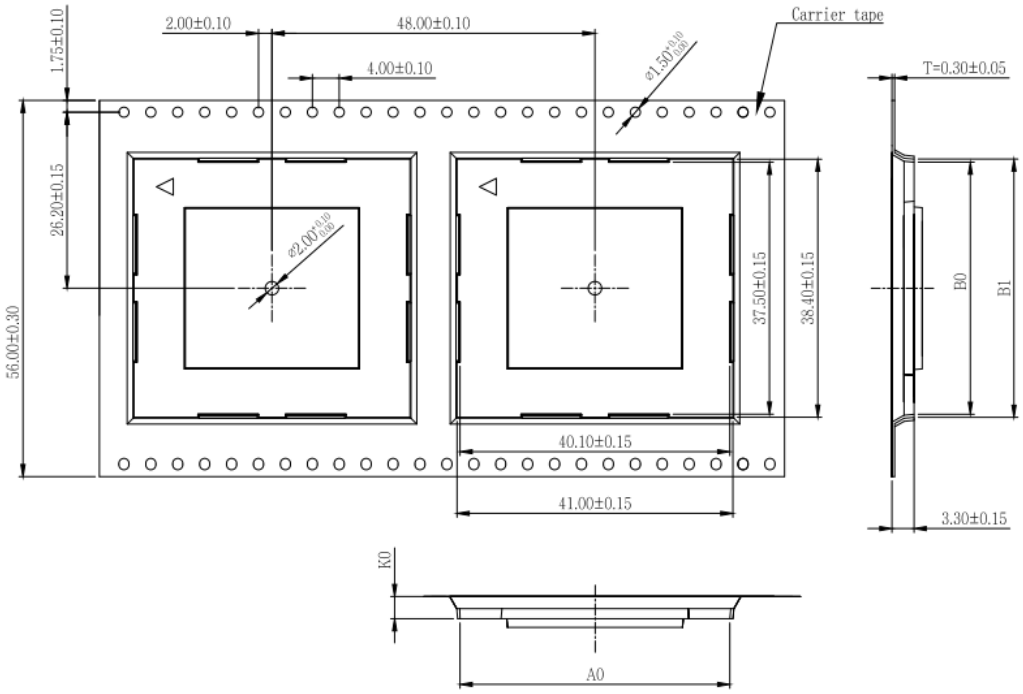


Figure 48: Tape Specifications (Unit: mm)

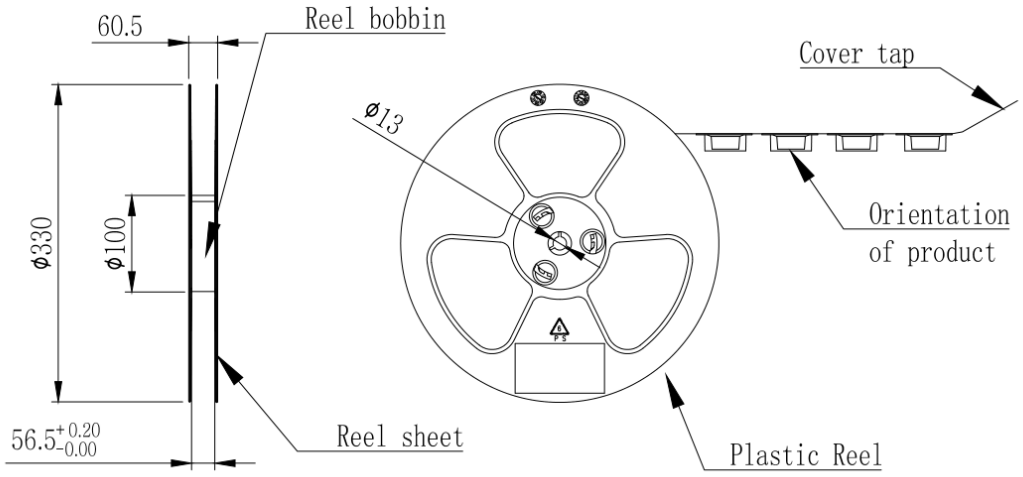


Figure 49: Reel Specifications (Unit: mm)

9 Appendix References

Table 49: Related Documents

SN	Document Name	Remark
[1]	Quectel_EP06&EG06&EM06_AT_Commands_Manual	AT Commands Manual for EP06, EG06 and EM06 Modules
[2]	Quectel_EP06&EG06&EM06_GNSS_AT_Commands_Manual	GNSS AT Commands Manual for EP06, EG06 and EM06 Modules
[3]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[4]	Quectel_EG06_Series_Reference_Design	EG06 Series Reference Design
[5]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[6]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal Design Guide for LTE Modules Including EC25, EC21, EC20 R2.0, EC20 R2.1, EG91, EG95, EP06, EG06, EM06 and AG35 modules

Table 50: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink

DTR	Data Terminal Ready
DTX	Discontinuous Transmission
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
I_{PP}	Peak Pulse Current
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMIC	Power Management IC
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RC Mode	Root Complex Mode
Rx	Receive
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
Tx	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value

V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network