EG060V-EA

Hardware Design

LTE-A Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-09-15	King MA/ Benjamin CHAI	Initial

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1 Introduction

This document defines the EG060V-EA module and describes its air and hardware interfaces which connect to your applications.

It familiarizes you with the module's interface specifications, electrical and mechanical details, as well as other related information. To facilitate application of the module in different fields, its reference designs are also provided for your reference. With this hardware design document, along with the application notes and user guides explicated therein, you can use the product to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG060V-EA module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

EG060V-EA, a type of LTE-FDD/LTE-TDD/WCDMA wireless communication module with receive diversity, provides data connectivity on LTE-FDD, LTE-TDD, HSPA+, HSDPA, HSUPA, and WCDMA networks.

Table 1: Frequency Bands of EG060V-EA Module

Mode	EG060V-EA
LTE-FDD (with Rx-diversity)	B1/B3/B5/B7/B8/B20/B28
LTE-TDD (with Rx-diversity)	B38/B40/B41
2 × CA [2)]	B1+B1/B3/B5/B8/B20/B28; B3+B3/B5/B7/B8 [1)]/B20/B28; B7+B5/B7/B8/B20/B28; B38+B38; B40+B40; B41+B41
WCDMA	B1/B5/B8

NOTES

1. [1)] For CA-3A-8A, “B3 (PCC) + B8 (SCC)” is supported, while “B8 (PCC) + B3 (SCC)” is not.
2. [2)] EG060V-EA supports continuous intra-band CA, but not non-continuous intra-band CA.

With a compact profile of 37.0 mm × 39.5 mm × 3.05 mm, EG060V-EA can meet almost all requirements for M2M applications, such as automotive applications, meters, tracking systems, security systems, routers, wireless POS systems, mobile computing devices, PDA phones, tablet PCs, etc.

EG060V-EA is an SMD type module which can be embedded into applications through its 299 LGA pins.

2.2. Key Features

The following table describes the detailed features of the module.

Table 2: Key Features of EG060V-EA Module

Feature	Details
Power Supply	Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V
Transmitting Power	Class 3 (24 dBm +1/-3 dB) for WCDMA bands Class 3 (23 dBm ±2 dB) for LTE-FDD bands [1)] Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Support up to Cat 6 FDD and TDD CA Support uplink QPSK and 16QAM modulation Support downlink QPSK, 16QAM and 64QAM modulation Support 1.4 MHz to 40 MHz (DL 2×CA) RF bandwidth Support 4 × 2, 2 × 2 MIMO in DL direction FDD: Max 300 Mbps (DL)/50 Mbps (UL) TDD: Max 220 Mbps (DL)/30 Mbps (UL)
UMTS Features	Support 3GPP R7 HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16QAM and 64QAM modulation HSDPA: Max 21 Mbps (DL) [2)] HSUPA: Max 5.76 Mbps (UL) WCDMA: Max 384 kbps (DL)/384 kbps (UL)
Internet Protocol Features	Support PPP/TCP/UDP/FTP/HTTP/NTP/PING/HTTPS/SMTP*/ MMS*/FTPS/SMTPS*/SSL protocols Support PAP and CHAP for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support (U)SIM card: 1.8/3.0 V
Audio Features	Support one digital audio interface: PCM interface WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support short frame synchronization Support master and slave modes

USB Interface	Compliant with USB 2.0 specifications, with maximum transmission rates up to 480 Mbps on USB 2.0. Used for AT command communication, data transmission, firmware upgrade, software debugging. Support USB serial drivers for: Windows 7/8/8.1/10; WinCE 5.0/6.0/7.0*; Linux 2.6/3.x/4.1–4.14; Android 4.x/5.x/6.x/7.x/8.x
UART Interfaces	**Main UART:** Used for AT command communication and data transmission Baud rate reaches up to 921600 bps, 115200 bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output 115200 bps baud rate
PCIe Interface*	Comply with PCI Express Specification Revision 1.0 Used for Ethernet or WLAN communication
Rx-diversity	Support LTE Rx-diversity
AT Commands	Compliant with *3GPP TS* 27.007, *3GPP TS* 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	Including the main antenna interface (ANT_MAIN) and Rx-diversity antenna interface (ANT_DRX)
Physical Characteristics	Size: (37.0 ±0.2) mm × (39.5 ±0.2) mm × (3.05 ±0.2) mm Weight: approx. 6.7 g
Temperature Range	Operating temperature range: -20 °C to +55 °C [3)] Extended temperature range: -25 °C to +60 °C [4)] Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface and FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] For LTE FDD Band 3, the transmitting power is 21.5 dBm ±1 dB.
2. [2)] DC-HSDPA can be used, but the throughput speed and connection stability has yet to be optimized.
3. [3)] Within operating temperature range, the module is 3GPP compliant.
4. [4)] Within extended temperature range, the module keeps the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There won't be unrecoverable malfunctions. Nor will there be effects on the radio spectrum or harm to radio networks. Only one or more parameters like P_{out} might reduce in the value and exceed specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
5. It is not recommended to use the module without adopting a heat dissipation component. Tests are

conducted at all temperature levels with heat sinks and rubber pads applied.

6. "*" means under development.

2.3. Functional Diagram

Below is the functional diagram of EG060V-EA with its major functional parts illustrated.

- Power management
- Baseband
- LPDDR (SDRAM) + NAND flash memory
- Radio frequency
- Peripheral interfaces

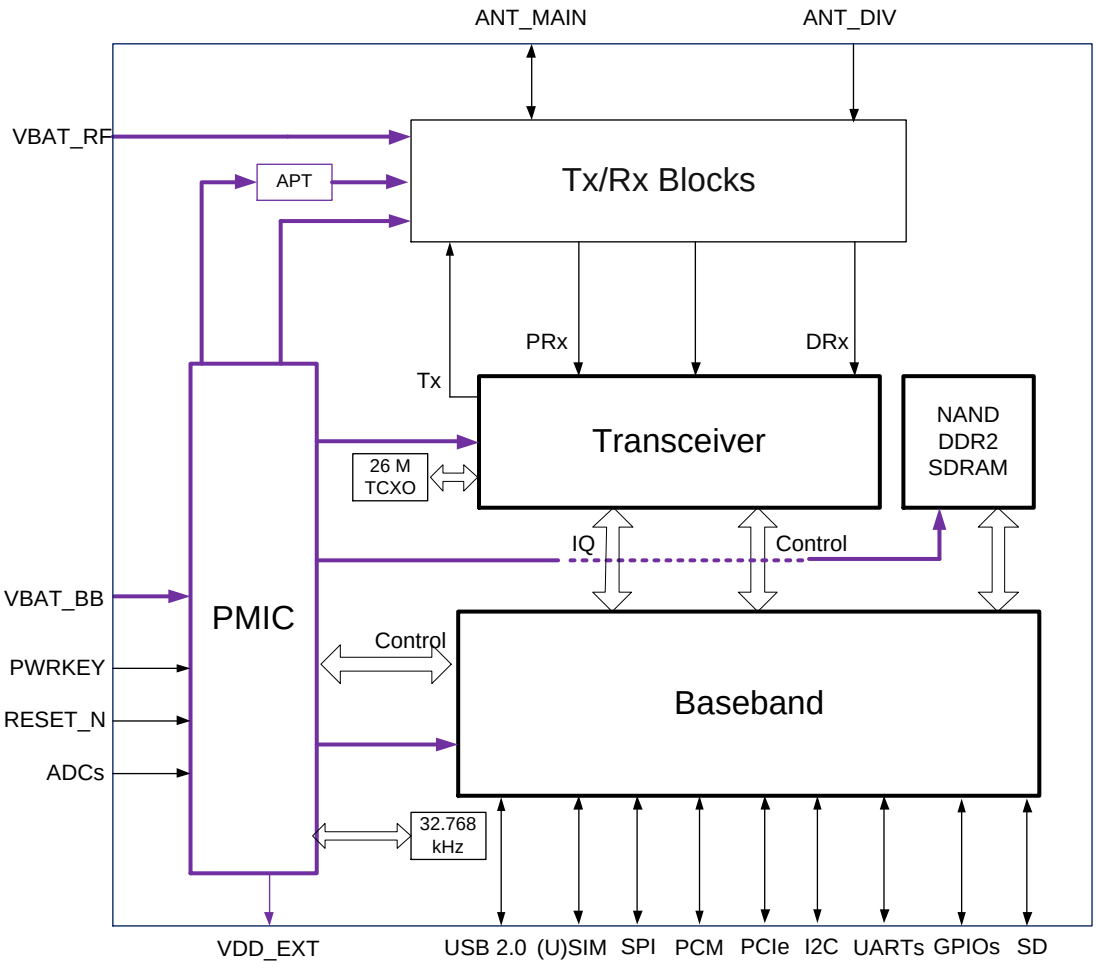


Figure 1: Functional Diagram

2.4. Evaluation Board

To help you develop applications handily with EG060V-EA, Quectel supplies an evaluation board (EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EG060V-EA is equipped with 299 LGA pins that can be connected to a cellular application platform. The following chapters describe the interfaces listed below.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- ADC interfaces
- Network indication Interfaces
- Module status indication Interface
- RI behaviors
- PCIe interface*
- WLAN control interface*
- SD card interface*
- SPI interface
- USB_BOOT interface

NOTE

"*" means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

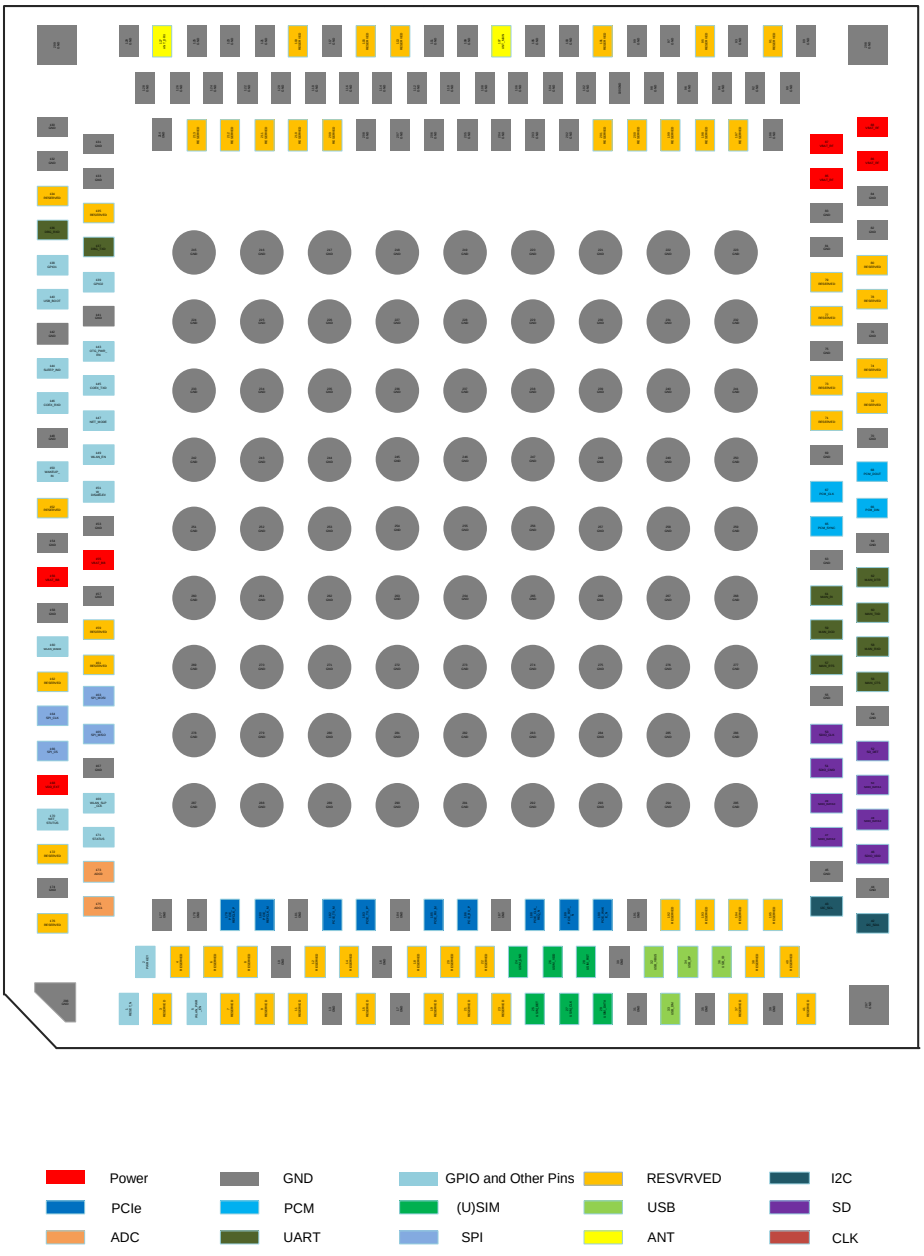


Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins disconnected.
2. GND pins 215–299 should be connected to ground in the design.

3.3. Pin Description

The following tables define and describe the pins of the module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155,156	PI	Power supply for the module's baseband part and RF part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with a sufficient current of 1.5 A at least.
VBAT_RF	85, 86, 87, 88	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with a sufficient current of 0.5 A at least [1].
VDD_EXT	168	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits.
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114, 116, 117, 118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191,196, 202–208, 214–299				

Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	2	DI	Turn on/off the module	V_{IH}max = 4.1 V V_{IH}min = 2.4 V V_{IL}max = 1.2 V	There is a pull-up power supply inside, no need to add any pull-up power supply outside.
RESET_N	1	DI	Reset the module	V_{IH}max = 2.0 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	
Module Status Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	171	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
Network Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	147	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_ STATUS	170	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	PI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	
USB_DP	34	IO	USB differential data (+)	Compliant with USB 2.0 standard specifications.	Require a differential impedance of 90 Ω.
USB_DM	33	IO	USB differential data (-)	Compliant with USB 2.0 standard specifications.	
USB_ID*	36	DI	USB ID detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. If unused, keep it open.

				V_{IH}max = 2.0 V	
OTG_PWR_EN*	143	DO	OTG power control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	24		Dedicated ground for (U)SIM card		
USIM_VDD	26	PO	(U)SIM card power supply	For 1.8 V (U)SIM: Vmax = 1.9 V Vmin = 1.7 V For 3.0 V (U)SIM: Vmax = 3.05 V Vmin = 2.75 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	29	IO	(U)SIM card data	For 1.8 V (U)SIM: V_{IL}max = 0.36 V V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.45 V For 3.0 V (U)SIM: V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_CLK	27	DO	(U)SIM card clock	For 1.8 V (U)SIM: V_{OL}max = 0.4 V V_{OH}min = 1.45 V For 3.0 V (U)SIM: V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_RST	28	DO	(U)SIM card reset	For 1.8 V (U)SIM: V_{OL}max = 0.4 V V_{OH}min = 1.45 V For 3.0 V (U)SIM: V_{OL}max = 0.4 V V_{OH}min = 2.3 V	
USIM_DET	25	DI	(U)SIM card	V_{IL}min = -0.3 V	1.8 V power domain.

			hot-plug detect	V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	61	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_DCD	59	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_CTS	56	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	57	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_DTR	62	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Pulling down to low level will wake up the module. If unused, keep it open.
MAIN_TXD	60	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	136	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	137	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it

					open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General-purpose ADC interface	Voltage range: 0 to 1.4 V	If unused, keep it open.
ADC1	175	AI	General-purpose ADC interface	Voltage range: 0 to 1.4 V	If unused, keep it open.
PCM and I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	66	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_DOUT	68	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	65	IO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	67	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C_SCL	43	OD	I2C serial clock (for external codec)	1.8 V power domain	An external pull-up resistor is required. 1.8 V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data (for external codec)	1.8 V power domain	An external pull-up resistor is required. 1.8 V only. If unused, keep it open.

SPI Interface [2)]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	166	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI_CLK	164	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI_MOSI	163	DO	SPI master-out	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI_MISO	165	DI	SPI master-in	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCIe Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)		If unused, keep it open.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)		If unused, keep it open.
PCIE_TX_M	182	AO	PCIe transmit (-)		If unused, keep it open.
PCIE_TX_P	183	AO	PCIe receive (+)		If unused, keep it open.
PCIE_RX_M	185	AI	PCIe receive (-)		If unused, keep it open.
PCIE_RX_P	186	AI	PCIe receive (+)		If unused, keep it open.
PCIE_CLKREQ_N	188	IO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_RST_N	189	IO	PCIe reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE_N	190	IO	PCIe wake up	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	In master mode, it is an input signal.

				V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	In slave mode, it is an output signal. If unused, keep it open.
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN	5	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_WAKE	160	DI	Wake up the host by an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active low. If unused, keep it open.
WLAN_EN	149	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. If unused, keep it open.
COEX_RXD	146	DI	LTE&WLAN coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
COEX_TXD	145	DO	LTE&WLAN coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If unused, keep it open.
SD Card Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	46	PO	SDIO power supply	For 1.8 V SD: Vmax = 1.9 V Vmin = 1.75 V For 3.0 V SD: Vmax = 3.05 V Vmin = 2.75 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically. Power supply for SD card must be provided by an external power supply.
SDIO_DATA0	49	IO	SDIO data bit 0	For 1.8 V SD: V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V	If unused, keep it open.
SDIO_DATA1	50	IO	SDIO data bit 1		If unused, keep it open.

SDIO_DATA2	47	IO	SDIO data bit 2	V_{IL}max = 0.58 V V_{IH}min = 1.3 V V_{IH}max = 2.0 V For 3.0 V SD: V_{OL}max = 0.35 V V_{OH}min = 2.15 V V_{IL}min = -0.3 V V_{IL}max = 0.7 V V_{IH}min = 1.8 V V_{IH}max = 3.15 V	If unused, keep it open.
SDIO_DATA3	48	IO	SDIO data bit 3		If unused, keep it open.
SDIO_CMD	51	DO	SD card command		If unused, keep it open.
SDIO_CLK	53	DO	SD card clock		If unused, keep it open.
SD_DET	52	DI	SD card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DRX	127	AI	Diversity antenna interface		50 Ω impedance. If unused, keep it open.
ANT_MAIN	107	IO	Main antenna interface		50 Ω impedance.
GPIO Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	138	IO	General purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep them open.
GPIO2	139	IO			
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	150	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. Bringing it LOW wakes up the module. If unused, keep it open.

W_DISABLE#	151	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. Bringing it LOW sets the module into airplane mode. If unused, keep it open.
USB_BOOT	140	DI	Force the module into emergency download mode.	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SLEEP_IND	144	DO	Indicate the module's sleep mode	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 4, 6, 7, 8, 9, 11, 12, 14, 15, 18–23, 37, 38, 40, 41,71–74, 77–80, 91, 95, 101, 113, 115, 119, 134, 135, 152, 159, 161, 162,172, 176, 192–195, 197–201,209–213 18–23, 37,38,40,41, 71–74,77–80,192–195, 197–201, 209–213				Keep these pins disconnected.

NOTES

1. [1] The current consumption is tested in 3G/4G instead of 2G environment.
2. [2] The SPI interface only supports master mode.
3. "*" means under development.

3.4. Operating Modes

The table below briefly summarizes the module's operating modes referred to in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	The module has registered on network and is ready to send and receive data, its software being active.
	Talk/Data	The module is connected to network, its power consumption decided by network setting and data transfer rate.

Minimum Functionality Mode	Executing **AT+CFUN=0** command can set the module into minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.
Airplane Mode	Executing **AT+CFUN=4** command or driving W_DISABLE# pin to low logic level can set the module into airplane mode where the RF function is invalid.
Sleep Mode	The module keeps receiving paging messages, SMS, voice calls and TCP/UDP data from the network, its current consumption reduced to the minimal level.
Power Down Mode	The module's power supply is cut off by its power management unit, its software being inactive and interfaces inaccessible while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.5. Power Saving

3.5.1. Sleep Mode

In the sleep mode, DRX, whose cycle index value is broadcasted via the wireless network, reduces the module's current consumption to a minimum level. The figure below shows the relationship between DRX run time and current consumption in this mode: the longer the DRX runs, the lower the current consumption.

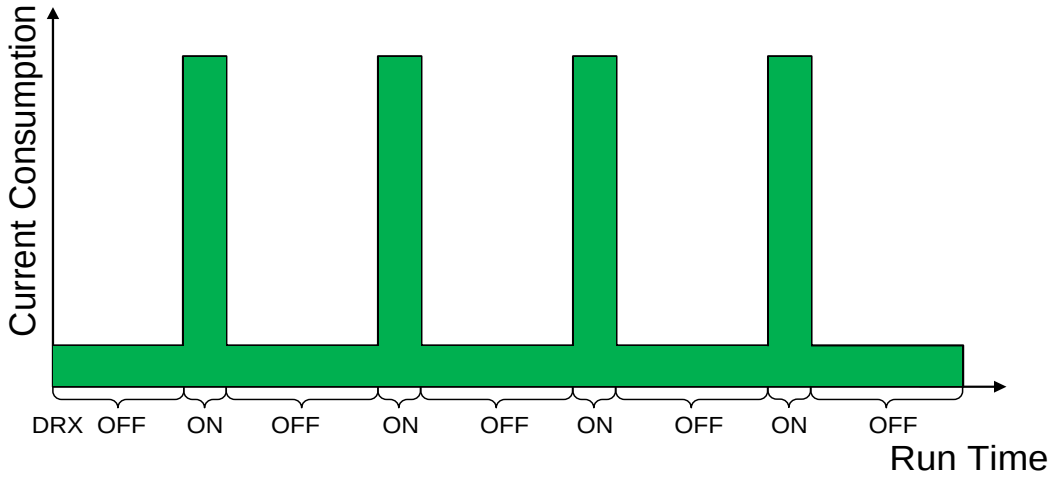


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following sections describe the different approaches to setting the module into sleep mode.

3.5.1.1. Set Sleep Mode via UART

If the host communicates with the module via UART interface, the following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive MAIN_DTR HIGH.

The following figure shows the connection between module and host in this case.

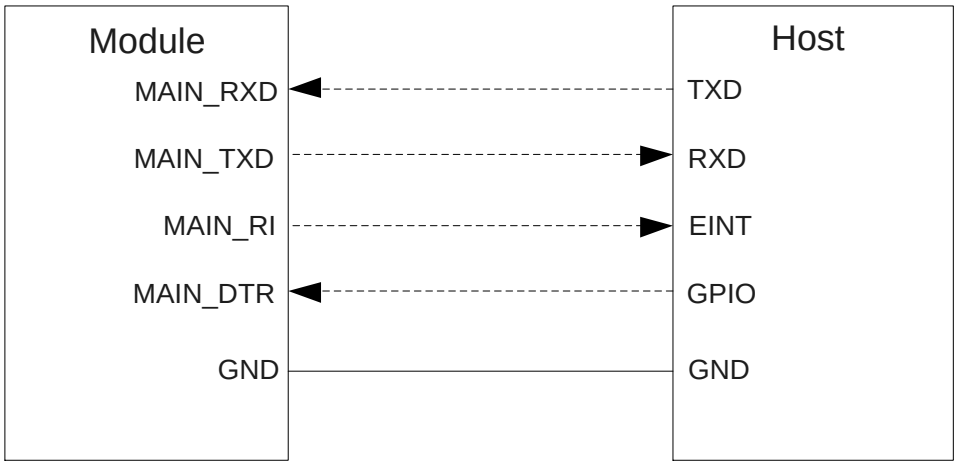


Figure 4: Set Sleep Mode via UART

The module and the host will be waken up in the following conditions:

- Driving the host DTR LOW will wake up the module.
- When the module has a URC to report, an RI signal will wake up the host. Please refer to ***Chapter 3.16*** for details about RI behavior.

3.5.1.2. Set Sleep Mode via USB with Suspend/Resume and Remote Wakeup

If the host supports USB suspend/resume and remote wakeup functions, the following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which connects to the module's USB interface, is in suspend mode.

The following figure shows the connection between module and host in this case.

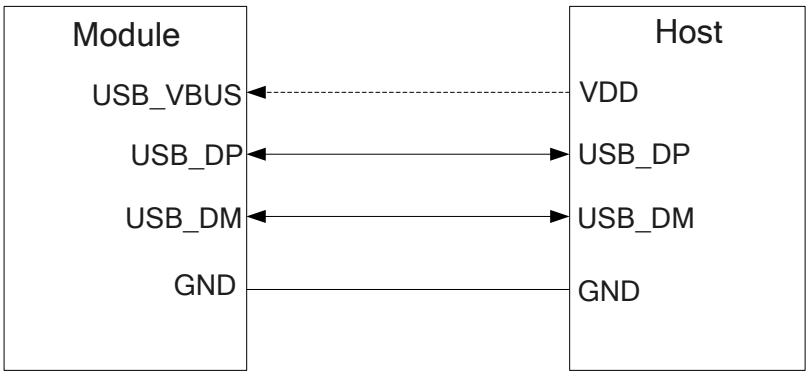


Figure 5: Sleep Mode with Remote Wakeup

The module and the host will be waken up in the following conditions:

- Sending data to EG060V-EA through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals to USB bus so as to wake up the host.

3.5.1.3. Set Sleep Mode via USB with Suspend/Resume and RI Function

If the host supports USB suspend/resume but not remote wake-up function, the RI signal is needed to wake up the host. The following steps are required to set the module into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which connects to the module's USB interface, is in suspend mode.

The following figure shows the connection between module and host in this case.

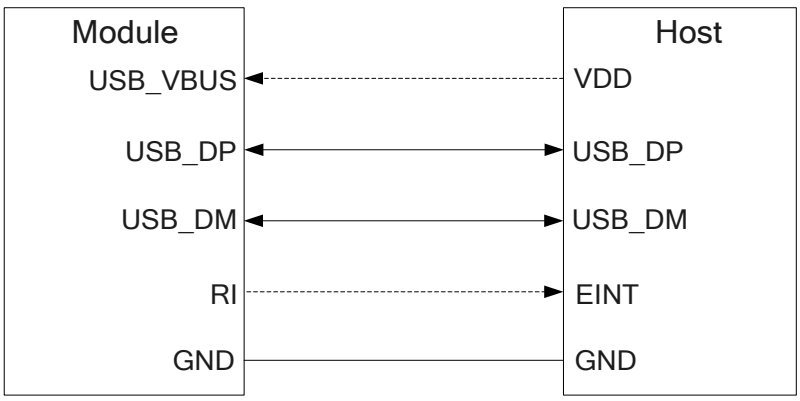


Figure 6: Sleep Mode with RI Signal Wakeup

The module and the host will be waken up in the following conditions:

- Sending data to EG060V-EA through USB will wake up the module.
- When the module has a URC to report, RI signal will wake up the host.

3.5.1.4. Set Sleep Mode via USB without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected from an external control circuit to enable the module to enter into sleep mode. The following steps are required to this end.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between module and host in this case.

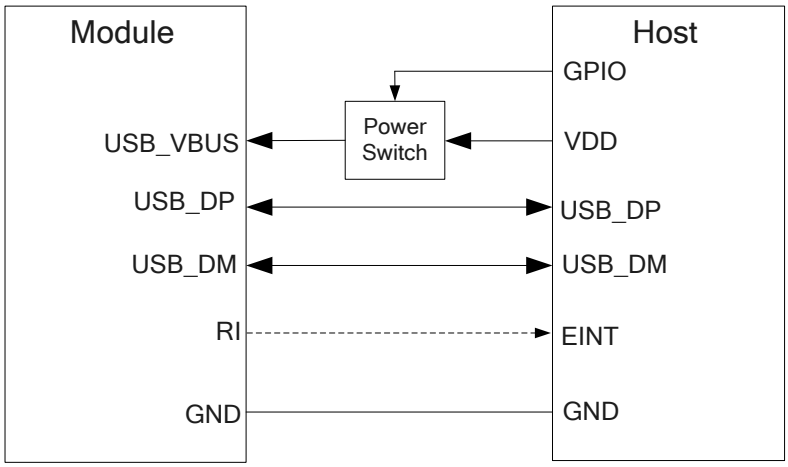


Figure 7: Sleep Mode without Suspend Function

Supply power to USB_VBUS with the power switch will wake up the module.

NOTE

Please pay attention to the level matching between module and host.

3.5.2. Airplane Mode

When the module is in airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible.

This mode can be set with the following approaches.

- **Hardware approach:**

  The W_DISABLE# pin is pulled up by default; driving it to low level will set the module into airplane mode.

- **Software approach:**

  AT+CFUN command provides the choice of functionality level through setting the value of **<fun>** to 0, 1 or 4.

  - **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
  - **AT+CFUN=1:** Full functionality mode (by default).
  - **AT+CFUN=4:** Airplane mode; RF function is disabled.

NOTE

The W_DISABLE# control function is disabled in firmware by default. It can be enabled by executing **AT+QCFG="airplanecontrol"** command, which is under development.

3.6. Power Supply

3.6.1. Power Supply Pins

EG060V-EA provides six VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for these pins.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part and RF part

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86 87, 88	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for the module's BB part and RF part	3.3	3.8	4.3	V

GND	10, 13, 16, 17, 24, 30,31, 35, 39,44, 45, 54, 55, 63, 64, 69, 70, 75,76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114, 116–118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3 to 4.3 V. Please make sure the input voltage never drops below 3.3 V. The following figure shows the voltage drop in case of burst transmission in 3G and 4G networks.

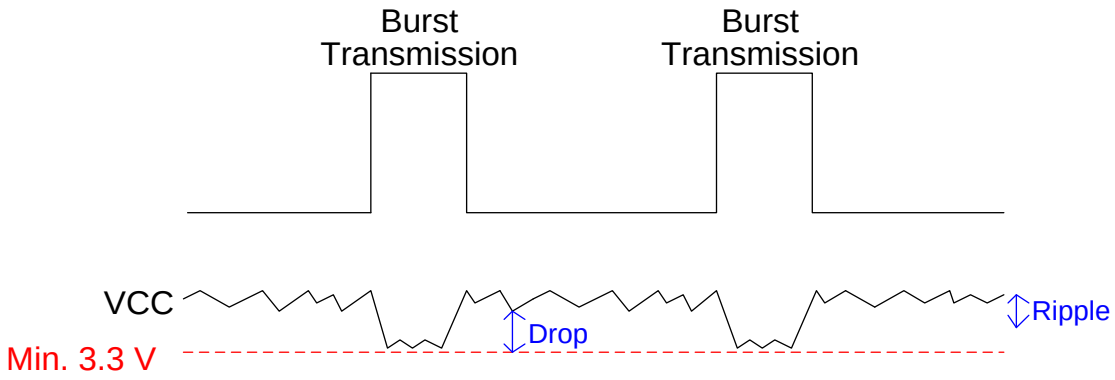


Figure 8: Voltage Drop Limits during Tx

To decrease the voltage drop, a bypass capacitor of about 100 µF with low ESR should be used, so does a multi-layer ceramic chip (MLCC) capacitor array for its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be the single voltage source which supplies power along two sub paths with star structure. The width of both VBAT_BB and VBAT_RF traces should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is recommended to use a TVS diode with suggested low-reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high-reverse peak pulse current I_{PP}.

The following figure shows the star structure of the power supply.

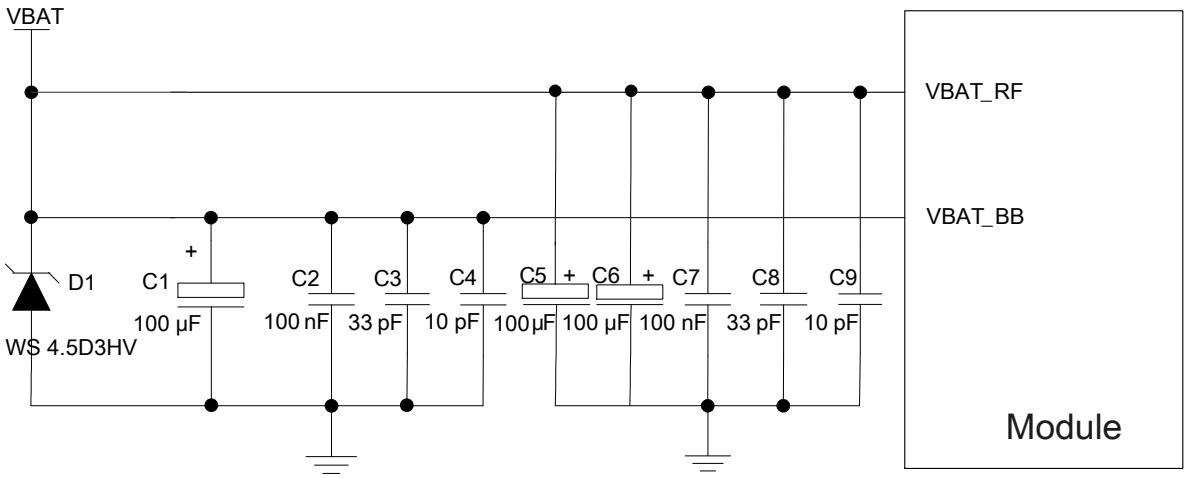


Figure 9: Star Structure of Power Supply

3.6.3. Reference Design of Power Supply

Power design is critical as the performance of the module largely depends on the stability and suitability of its power source. The power supply of EG060V-EA should be able to provide a sufficient current of 2 A [1)] at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used while supplying power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred.

The following figure shows a reference design for a +5 V input power source. The designed output of the power supply is about 3.8 V and the maximum load current is 3 A.

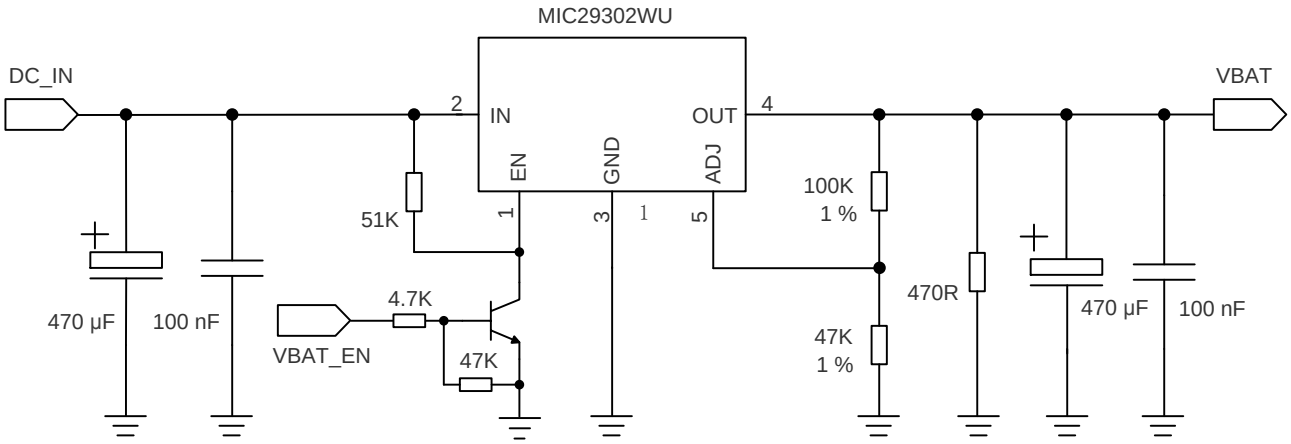


Figure 10: Reference Design of Power Supply

NOTES

1. To avoid damaging the internal flash, please do not cut off power supply when the module works normally. Only after the module is shut down with PWRKEY or AT command can the power supply be cut off.
2. [1)] The current consumption is tested in 3G/4G instead of 2G environment.

3.6.4. Monitor Power Supply

AT+CBC command can be used to monitor the voltage value of VBAT_BB. For more details, please refer to ***document [1]***.

3.7. Turn on/off

3.7.1. Turn on the Module with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	2	Turn on/off the module	V_{IH}max = 4.1 V V_{IH}min = 2.4 V V_{IL}max = 1.2 V	There is a pull-up power supply inside, no need to add any pull-up power supply outside.

When EG060V-EA is in power down mode, you can set it into normal mode by driving the PWRKEY pin to a low level for at least 500ms, advisably using an open collector driver, and release the pin after the STATUS pin outputs high level. A reference design is given below.

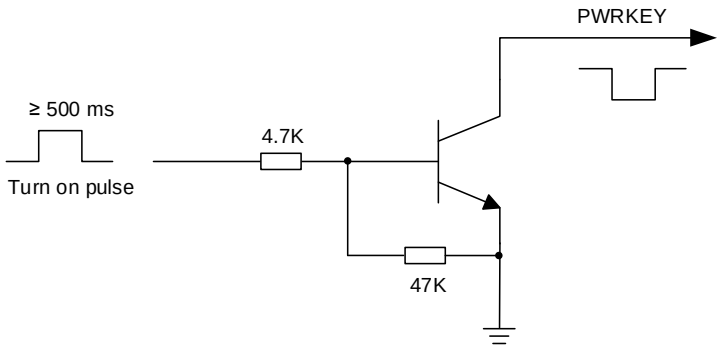


Figure 11: Turn on the Module with Driving Circuit

Another way to control the PWRKEY pin is by using a button. To protect your finger from electronic strikes when you press the key, a TVS component placed near the button for ESD protection is indispensable. A reference design is given below.

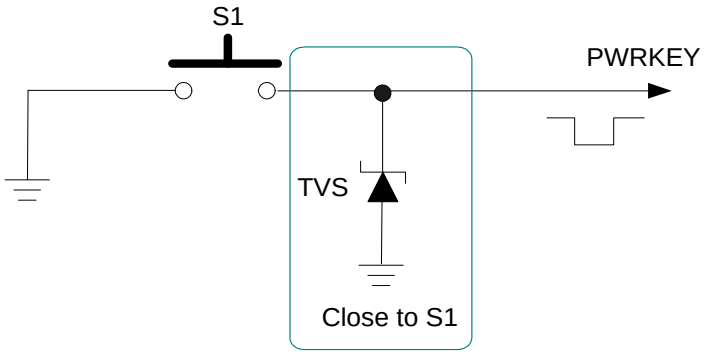


Figure 12: Turn on the Module with Button

The timing of turning on is illustrated in the following figure.

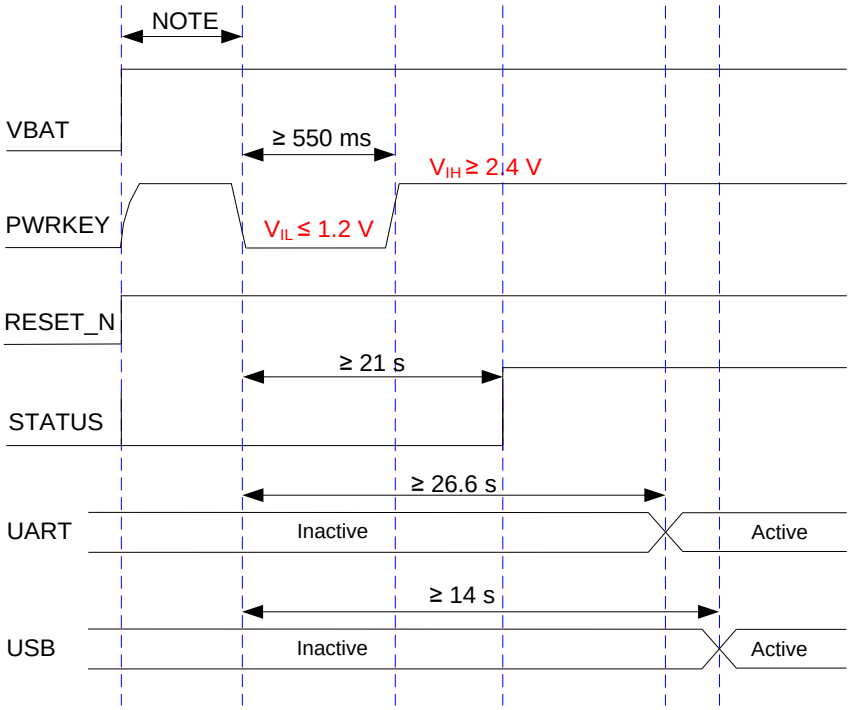


Figure 13: Timing of Turning on the Module

NOTE

Please make sure that VBAT is stable for no less than 300 ms before pulling down the PWRKEY pin.

3.7.2. Turn off the Module

Normally, there are two approaches to turning off the module:

- Turn off the module using the PWRKEY pin.
- Turn off the module using **AT+QPOWD** command.

3.7.2.1. Turn off the Module with PWRKEY

Driving the PWRKEY pin to a low level for at least 800 ms, and the module will power off after the pin is released. The timing of turning off the module is illustrated in the following figure.

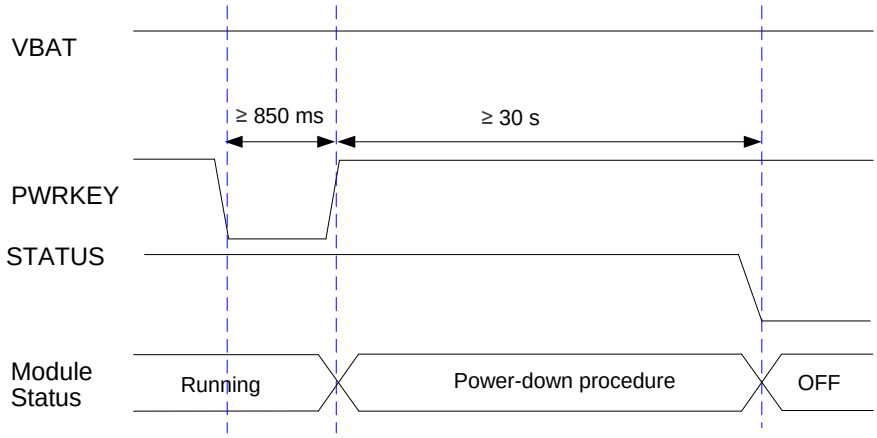


Figure 14: Timing of Turning off the Module

3.7.2.2. Turn off the Module with AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via the PWRKEY pin. Please refer to ***document [1]*** for details about the **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off the module with AT command, please keep the PWRKEY at high level after executing the power-off command. Otherwise the module will power on again after its being turned off.

3.8. Reset the Module

The module can be reset by driving RESET_N LOW for 250–600 ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	1	Reset the module	V_{IH}max = 2.0 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	

The recommended circuit is similar to the PWRKEY control circuit. An open collector driver or button can be used to control the RESET_N.

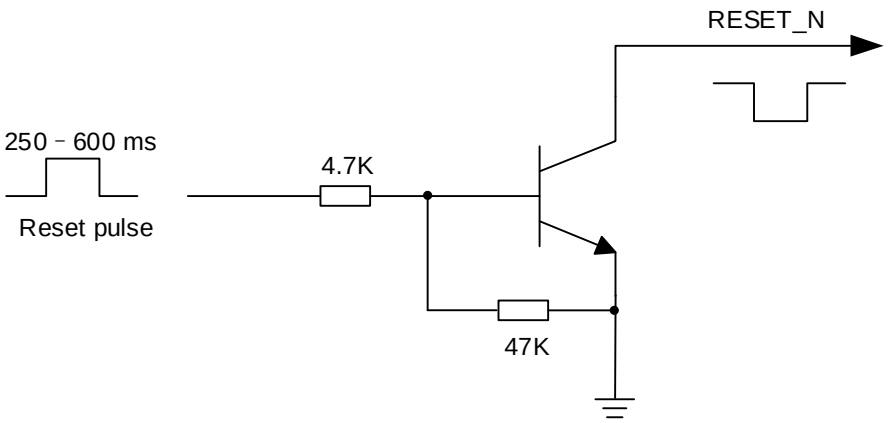


Figure 15: Resetting the Module with Driving Circuit

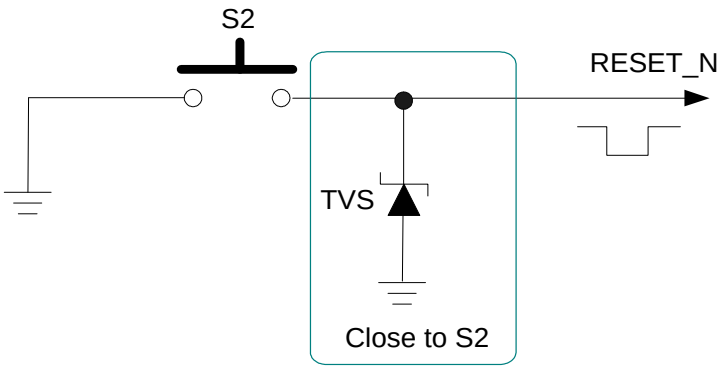


Figure 16: Resetting the Module with Button

The timing of reset is illustrated in the following figure.

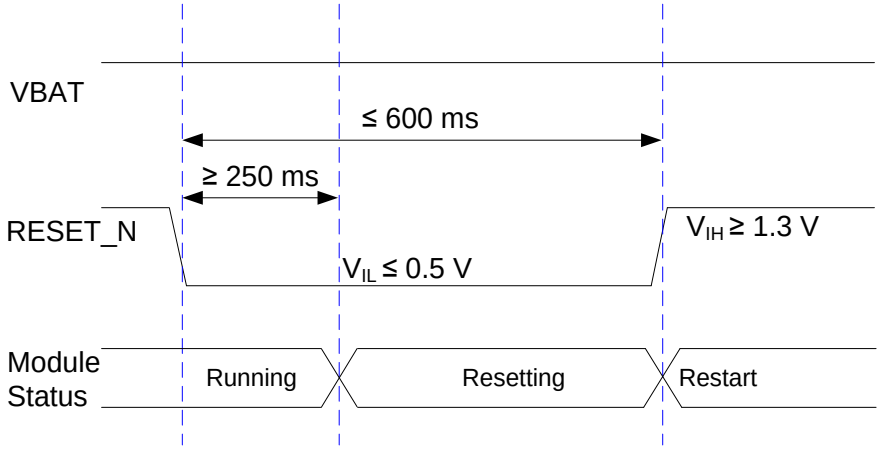


Figure 17: Timing of Resetting the Module

NOTES

1. Reset the module with RESET_N pin only when the module fails to be turned off by **AT+QPOWD** command or the PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM cards is supported.

Table 9: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	26	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	29	IO	(U)SIM card data	
USIM_CLK	27	DO	(U)SIM card clock	
USIM_RST	28	DO	(U)SIM card reset	
USIM_DET	25	DI	(U)SIM card hot-plug detect	

USIM_GND	24	Dedicated ground for (U)SIM card

The module supports (U)SIM card hot-plug via the USIM_DET pin. The function, which supports low-level and high-level detections, is disabled by default. Please refer to ***document [1]*** about **AT+QSIMDET** command for details.

Below is a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

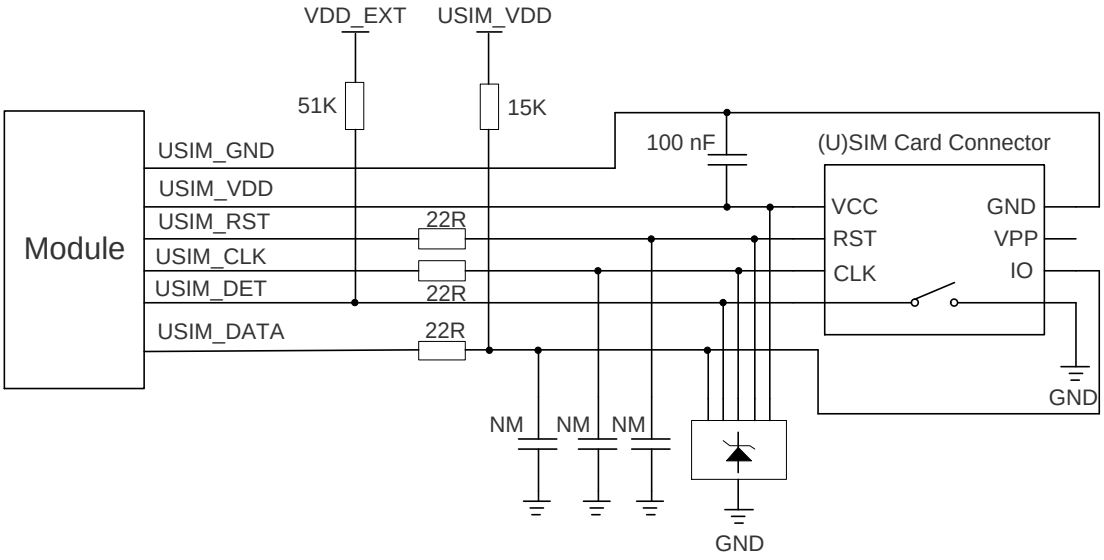


Figure 18: Reference Design of (U)SIM Interface with 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET disconnected. A reference design for (U)SIM interface with a 6-pin (U)SIM card connector is shown below.

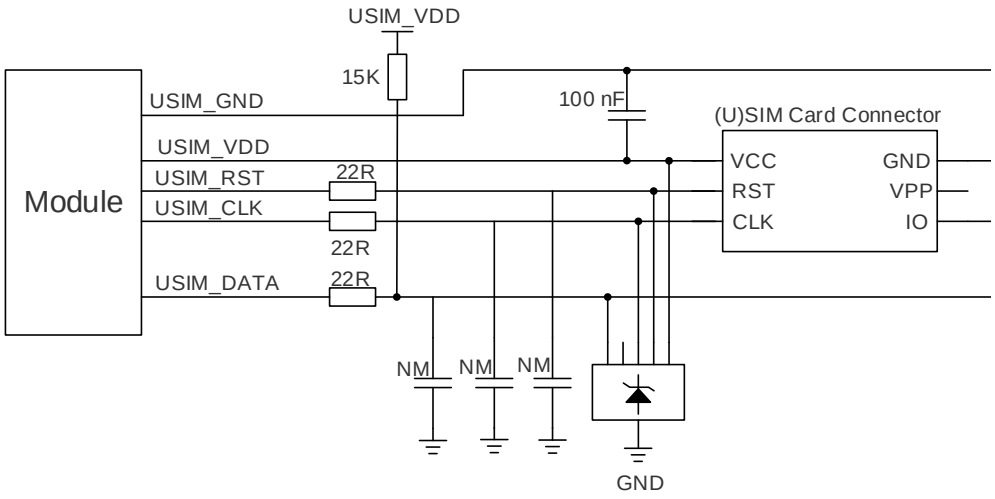


Figure 19: Reference Design of (U)SIM Interface with 6-Pin (U)SIM Card Connector

In order to enhance the reliability and usability of the (U)SIM card in use, please follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make the ground between module and (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to avoid any decrease in electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS diode array whose parasitic capacitance is within 15 pF. To facilitate debugging, add 22 ohm resistors in series between module and (U)SIM card. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability in sensitive occasions or when long traces are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG060V-EA provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface can only serve as a slave component and is used for AT command communication, data transmission, software debugging and firmware upgrading.

The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	34	IO	USB 2.0 differential data (+)	Require a differential impedance of 90 Ω
USB_DM	33	IO	USB 2.0 differential data (-)	
USB_VBUS	32	PI	USB connection detect	Typical 5.0 V
USB_ID*	36	DI	USB ID detect	
OTG_PWR_EN*	143	DO	OTG power control	
GND	35		Ground	

For more details about the specifications of USB 2.0, please visit this website down below:

https://www.usb.org/document-library/usb-20-specification.

It is recommended to reserve in your designs the USB interface for firmware upgrades. Below is a reference design of USB 2.0 interface.

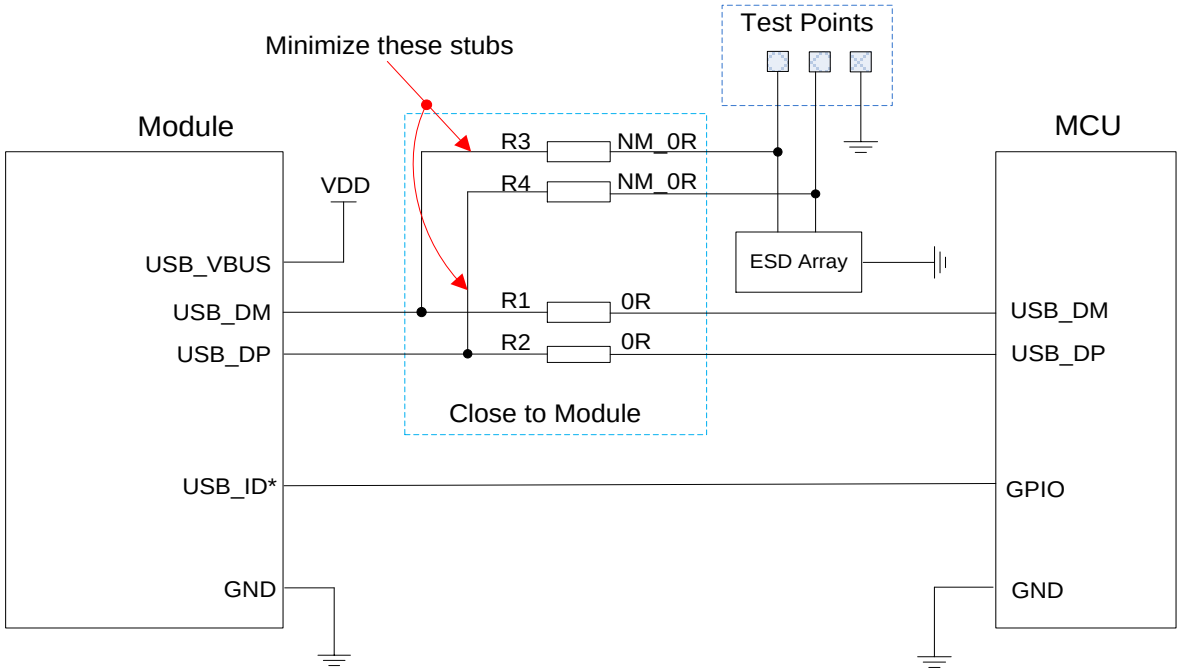


Figure 20: Reference Design of USB Interface

In order to ensure the signal integrity of USB data lines, R1, R2, R3 and R4 should be placed close to the module as well as to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specifications, the following principles should be complied with while designing the USB interface:

- It is important to route the USB signal traces as a differential pair with total grounding. Keep the impedance of the pair at 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on the same layer and with ground planes on adjacent layers.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data traces. Typically, the capacitance value of ESD protection components should be less than 2.0 pF for USB 2.0.
- Keep the ESD protection components as close to the USB connector as possible.
- If possible, reserve a 0 ohm resistor on USB_DP and USB_DM lines respectively.

NOTE

"*" means under development.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. Their features are shown below:

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default baud rate is 115200 bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition.

Table 11: Pin Definition of the Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	61	DO	Main UART ring indication	1.8 V power domain
MAIN_DCD	59	DO	Main UART data carrier detect	1.8 V power domain
MAIN_CTS	56	DO	Main UART clear to send	1.8 V power domain
MAIN_RTS	57	DI	Main UART request to send	1.8 V power domain
MAIN_DTR	62	DI	Main UART data terminal ready	1.8 V power domain
MAIN_TXD	60	DO	Main UART transmit	1.8 V power domain
MAIN_RXD	58	DI	Main UART receive	1.8 V power domain

Table 12: Pin Definition of the Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	137	DO	Debug UART transmit	1.8 V power domain

DBG_RXD	136	DI	Debug UART receive	1.8 V power domain

The logic levels are described in the following table.

Table 13: Logic Level Parameters of Digital I/O

Item	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. Below is a reference design.

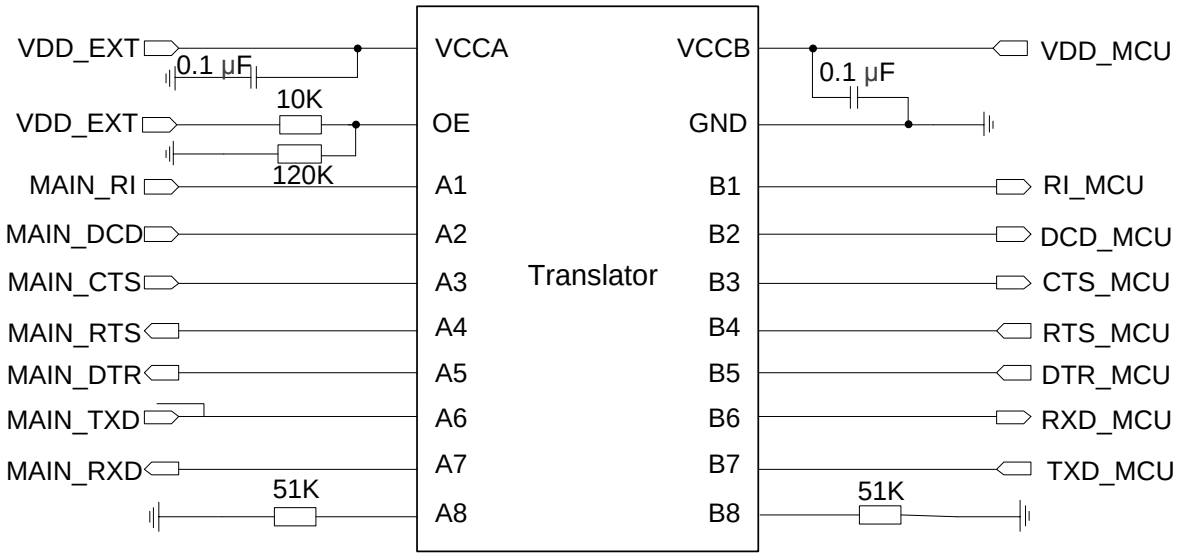


Figure 21: Reference Design of Translator Chip

Please visit http://www.ti.com for more information on the recommended translator.

Another approach to level translation is with a transistor translation circuit. A reference design in this regard is shown below. For the design of circuits shown by dotted lines, both input and output circuit designs, refer to the circuits shown by the solid lines, but please pay attention to the direction of connection.

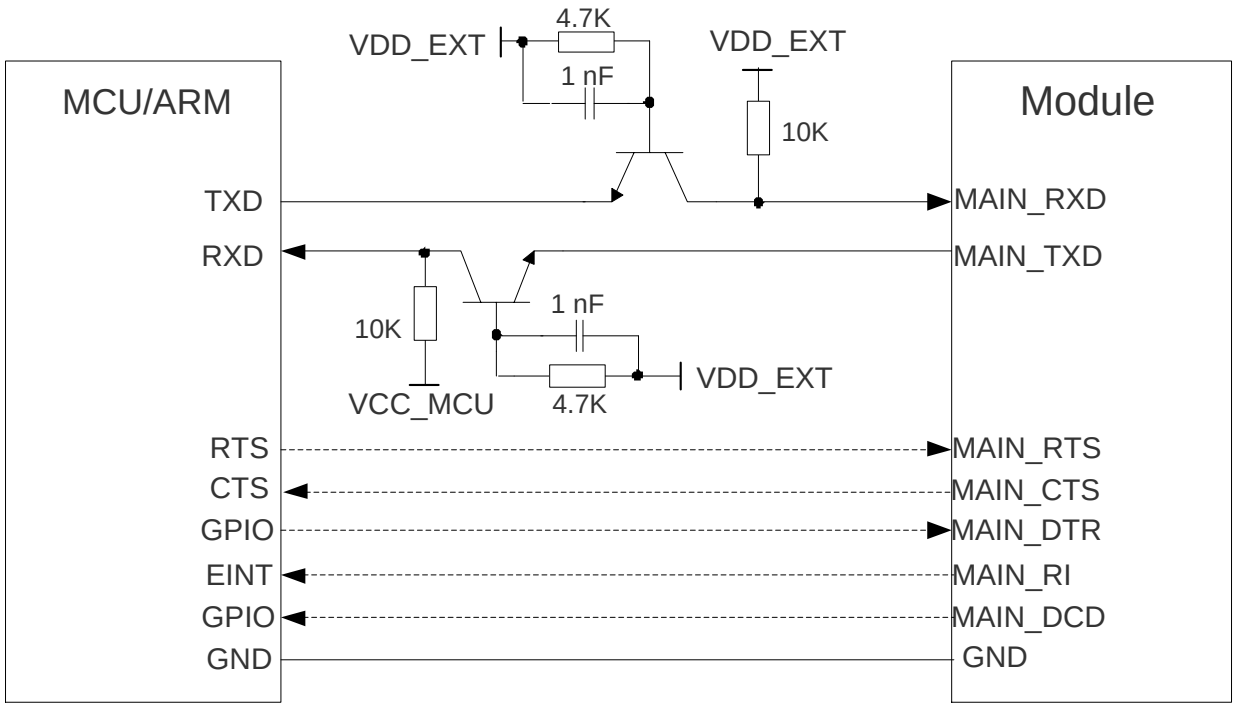


Figure 22: Reference Design of Transistor Circuit

NOTES

1. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module MAIN_CTS and MAIN_RTS are connected respectively to the host CTS and RTS.

3.12. PCM and I2C Interfaces

EG060V-EA supports audio communication via Pulse Code Modulation (PCM) digital interface and I2C interface.

The PCM interface supports the following mode:

- Primary mode (short frame synchronization): the module works as both master and slave.

In the primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The module supports 16-bit linear data format. The following figures show the relationship between 8 kHz PCM_SYNC and 2048 kHz PCM_CLK in the primary mode.

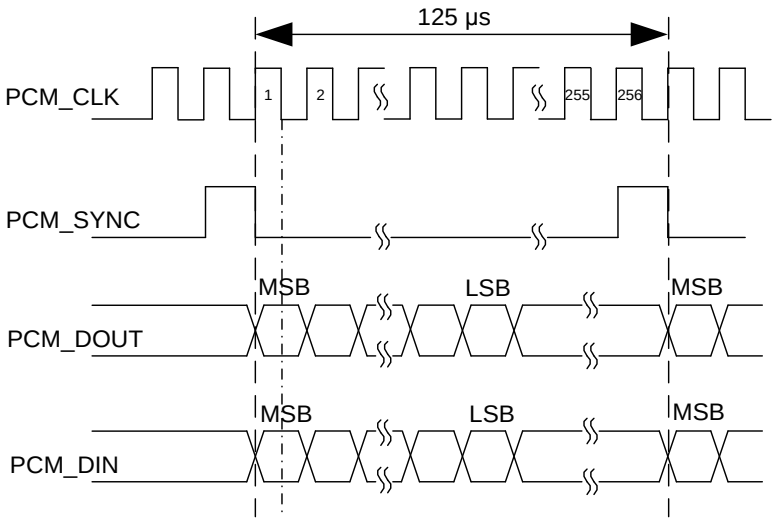


Figure 23: Primary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	66	DI	PCM data input	1.8 V power domain. If unused, keep it open.
PCM_DOUT	68	DO	PCM data output	1.8 V power domain. If unused, keep it open.
PCM_SYNC	65	IO	PCM data frame sync	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	67	IO	PCM clock	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C_SCL	43	OD	I2C serial clock (or external codec)	Needs to be pulled up to 1.8 V.
I2C_SDA	42	OD	I2C serial data (for external codec)	

Clock and mode can be configured by AT command, and the default configuration is master mode using

short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. Please refer to **AT+QDAI** command in ***document [1]*** for details.

The following figure shows a reference design of PCM interface with an external codec IC.

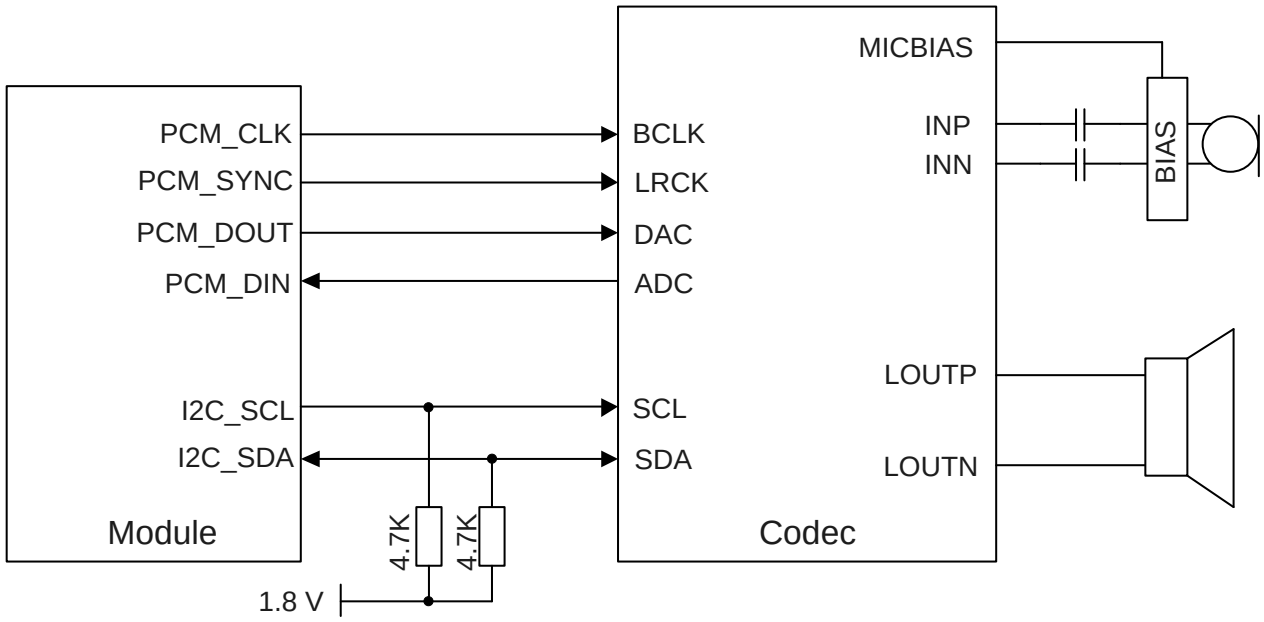


Figure 24: Reference Design of PCM Interface with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG060V-EA works as a master device pertaining to I2C interface.

3.13. ADC Interfaces

The module provides two Analog-to-Digital Converters (ADC) interfaces. **AT+QADC=0** command and **AT+QADC=1** command can be used respectively to read the voltage value on ADC0 pin and ADC1 pin. For more details about these **AT+QADC** commands, please refer to ***document [1]***.

In order to improve the accuracy of reading, the trace of ADC should be surrounded by ground.

Table 15: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	DC Characteristics
ADC0	173	General-purpose ADC interface	Voltage range: 0 to 1.4 V
ADC1	175	General-purpose ADC interface	

The following table describes the characteristics of the ADC interfaces.

Table 16: Parameters of ADC Interfaces

Item	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0		1.4	V
ADC1 Voltage Range	0		1.4	V
ADC Resolution		12		bits

NOTES

1. The input voltage of ADC should not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use a resistor divider for ADC application.

3.14. Network Indication Interface

The network mode/status indication pins, NET_MODE and NET_STATUS, can be used to drive network status indication LEDs; Their definitions and logic level changes upon the switch of network mode/status are described in the following tables.

Table 17: Pin Definition of Network Mode/Status Indication Pins

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	1.8 V power domain
NET_STATUS	170	DO	Indicate the module's network activity status	1.8 V power domain

Table 18: Working State of Network Mode/Status Indication Pins

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Other circumstances
NET_STATUS	LEDs flicker slowly (200 ms High / 1800 ms Low)	Network searching
	LEDs flicker slowly (1800 ms High / 200 ms Low)	Idle
	LEDs flicker quickly (125 ms High / 125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

Below is a reference design of the network indicator.

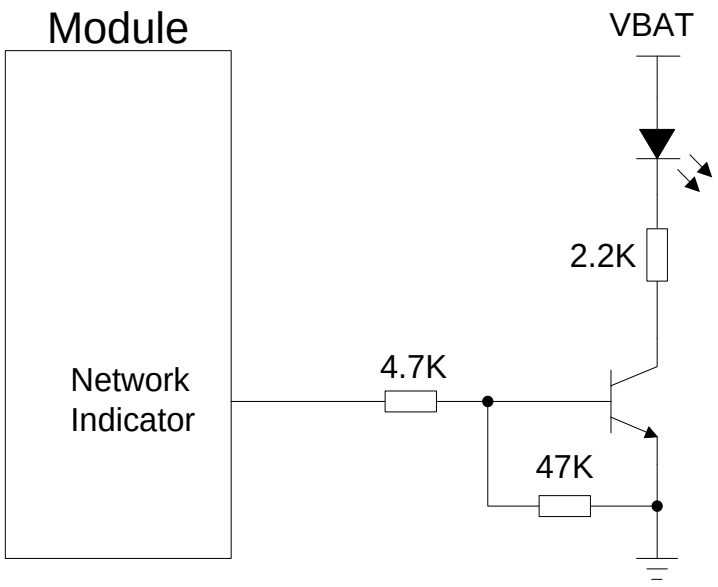


Figure 25: Reference Design of Network Indicator

3.15. Module Status Indication Interface

The STATUS pin is used to indicate the module's on or off status; It outputs high level when the module is turned on.

The following table describes the pin definition of STATUS.

Table 19: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	1.8 V power domain

Below is a reference design of the pin.

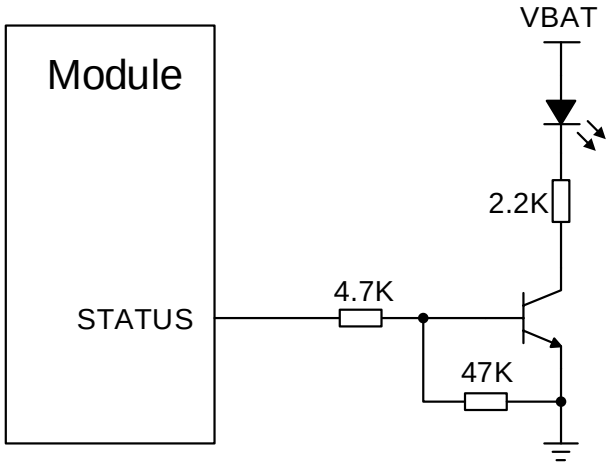


Figure 26: Reference Design of STATUS

3.16. RI Behaviors

The **AT+QCFG="risignaltype","physical"** command can be used to configure RI behavior.

Regardless of from which port a URC is output, it triggers the behavior of the RI pin.

NOTE

The URC can be output from UART port, USB AT port or USB modem port depending on the parameters of **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behavior of RI is shown below.

Table 20: Behavior of RI

State	Response
Idle	RI stays at high level
URC	RI outputs 120 ms low pulse when a new URC returns.

The RI behavior can be changed by the **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [1]*** for details.

3.17. PCIe Interface*

EG060V-EA provides a PCIe interface which is compliant with PCI Express Specification Revision 1.0. The key features of the PCIe interface are shown below:

- PCI Express Specification Revision 1.0 compliance
- Data rate reaching 2.5 Gbps per lane
- Connection to an external Ethernet IC (MAC and PHY) or WLAN IC.

The following table shows the pin definition of PCIe interface.

Table 21: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	179	AO	Output PCIe reference clock (+)	If unused, keep it open.
PCIE_REFCLK_M	180	AO	Output PCIe reference clock (-)	If unused, keep it open.
PCIE_TX_M	182	AO	PCIe transmit (-)	If unused, keep it open.
PCIE_TX_P	183	AO	PCIe transmit (+)	If unused, keep it open.
PCIE_RX_M	185	AI	PCIe receive (-)	If unused, keep it open.
PCIE_RX_P	186	AI	PCIe receive (+)	If unused, keep it open.
PCIE_CLKREQ_N	188	IO	PCIe clock request	In master mode, it is an input signal. In slave mode, it is an output signal.

				If unused, keep it open.
PCIE_RST_N	189	IO	PCIe reset	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE_N	190	IO	PCIe wake up	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.

In order to enhance the module's reliability and usability in applications, please follow the criteria below in PCIe interface circuit design:

- Keep PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and 19.2 MHz clock signals.
- A capacitance should be added in series on Tx/Rx traces to remove any DC bias.
- Keep the maximum trace length less than 300 mm.
- The length difference of the Tx or Rx differential pair of PCIe traces should be less than 0.7 mm.
- The differential impedance of PCIe data traces should be 100 Ω ±10 %.
- PCIe data traces must not be routed under components or crossing other traces.

NOTE

"*" means under development.

3.18. WLAN Control Interface*

EG060V-EA provides a low power PCIe interface* and a control interface for WLAN design. The following table shows the pin definition of WLAN control interface.

Table 22: Pin Definition of WLAN Control Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_PWR_EN	5	DO	WLAN power supply enable control	1.8 V power domain
WLAN_WAKE	160	DI	Wake up the host by an external Wi-Fi module	1.8 V power domain
WLAN_EN	149	DO	WLAN function enable control	1.8 V power domain
COEX_RXD	146	DI	LTE&WLAN coexistence receive	1.8 V power domain

COEX_TXD	145	DO	LTE&WLAN coexistence transmit	1.8 V power domain
WLAN_SLP_CLK	169	DO	WLAN sleep clock	1.8 V power domain

NOTE

"*" means under development.

3.19. SD Card Interface*

EG060V-EA provides one SD card interface which supports SD 3.0 protocol. The following table shows the pin definition.

Table 23: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_DATA3	48	IO	SDIO data bit 3	
SDIO_DATA2	47	IO	SDIO data bit 2	
SDIO_DATA1	50	IO	SDIO data bit 1	
SDIO_DATA0	49	IO	SDIO data bit 0	
SDIO_CLK	53	DO	SD card clock	
SDIO_CMD	51	IO	SD card command	
SDIO_VDD	46	PO	SDIO power supply	1.8/2.85 V configurable output. Cannot be used for SD card power supply.
SD_DET	52	DI	SD card hot-plug detect	

Below is a reference design of the SD card interface of the module.

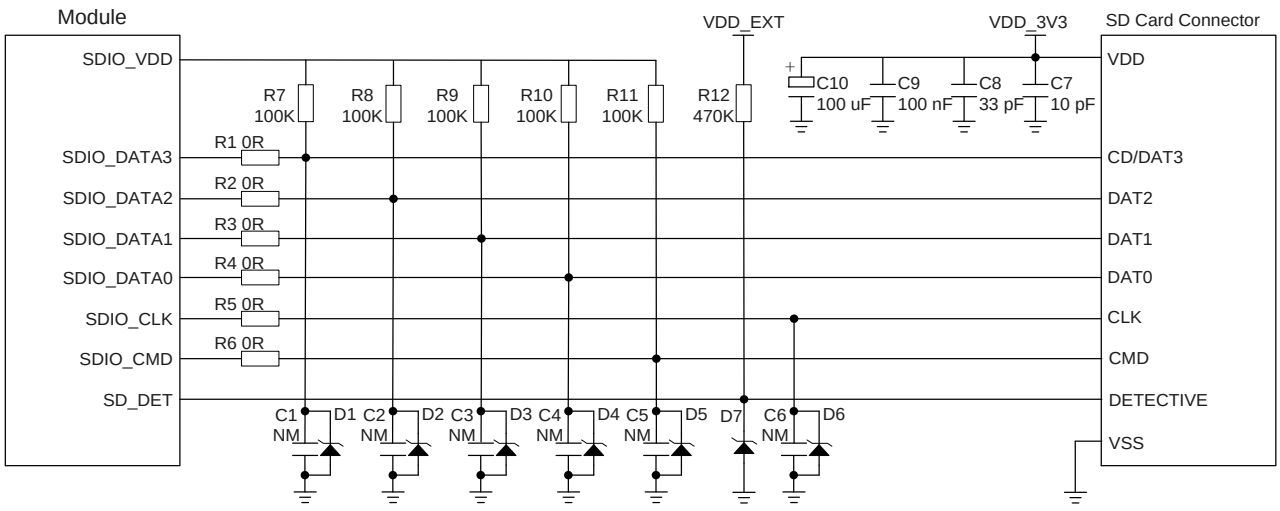


Figure 27: Reference Design of SD Card Interface

Please follow the principles below in SD card circuit design:

- The voltage range of SD power supply VDD_3V3 is 2.7–3.6 V and a sufficient current of 0.8 A at least should be provided. As the maximum output current of VDD_SDIO is 50 mA, which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SDIO_VDD. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ.
- In order to improve signal quality, it is recommended to add 0 ohm resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins.
- The load capacitance of SDIO bus needs to be less than 40 pF.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals, such as RF circuits, analog signals, etc., as well as noisy signals, such as clock signals, DCDC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 36 mm, so the exterior total trace length should be less than 14 mm.
- Make sure the spacing between adjacent traces is two times of the trace width and that the load capacitance of SDIO bus is less than 40 pF.

NOTE

"*" means under development.

3.20. SPI Interface

EG060V-EA provides one SPI interface which only supports master mode with a maximum clock frequency up to 50 MHz.

The following table shows the pin definition of SPI interface.

Table 24: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	166	DO	SPI chip select	1.8 V power domain. If unused, keep them open.
SPI_MOSI	163	DO	SPI master-out	
SPI_MISO	165	DI	SPI master-in	
SPI_CLK	164	DO	SPI clock	

The figure below shows the timing of SPI interface. The related parameters of SPI timing are shown in the following table.

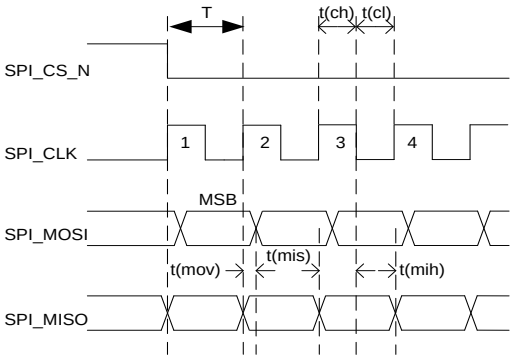


Figure 28: SPI Interface Timing

Table 25: Parameters of SPI Interface Timing

Item	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns

t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

The voltage range of the SPI interface is 1.8 V. Therefore, A level translator between module and host should be used if the application is equipped with a 3.3 V processor or device interface.

Below is a reference design of SPI Interface with a Level Translator.

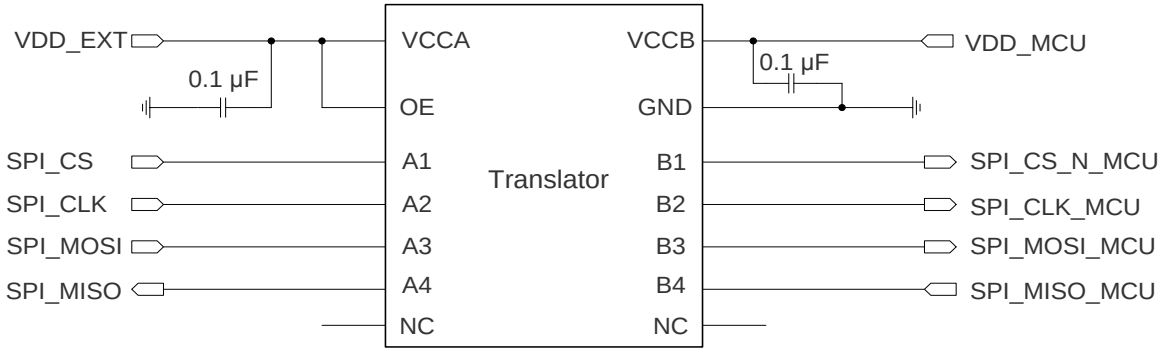


Figure 29: Reference Design of SPI Interface with Level Translator

3.21. USB_BOOT Interface

EG060V-EA provides a USB_BOOT interface. Developers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 26: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

Below is a reference design of USB_BOOT interface.

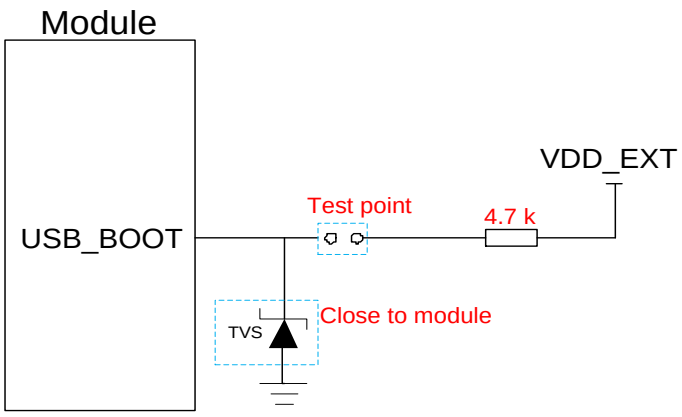


Figure 30: Reference Design of USB_BOOT Interface

4 Antenna Interfaces

EG060V-EA provides a main antenna interface and an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect. The impedance of antenna ports is 50 Ω.

4.1. Main/Rx-diversity Antenna Interface

4.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces are shown as below.

Table 27: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	107	IO	Main antenna interface	50 Ω impedance
ANT_DRX	127	AI	Diversity antenna interface	50 Ω impedance

4.1.2. Operating Frequency

Table 28: EG060V-EA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE B1	1920–1980	2110–2170	MHz
LTE B3	1710–1785	1805–1880	MHz
LTE B5	824–849	869–894	MHz

LTE B7	2500–2570	2620–2690	MHz
LTE B8	880–915	925–960	MHz
LTE B20	832–862	791–821	MHz
LTE B28	703–748	758–803	MHz
LTE B38	2570–2620	2570–2620	MHz
LTE B40	2300–2400	2300–2400	MHz
LTE B41	2496–2690	2496–2690	MHz

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DRX antenna interface is shown below. It should reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

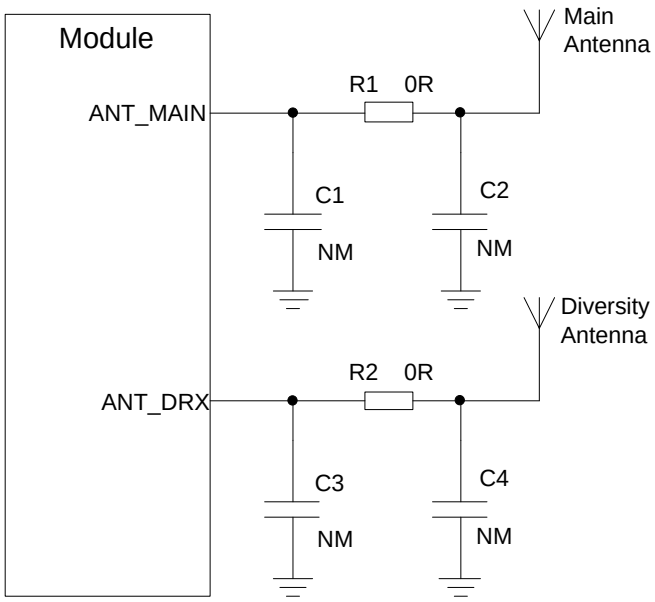


Figure 31: Reference Design of RF Antenna Interface

NOTES

1. Keep a proper distance between the main and the Rx-diversity antenna to improve the receiving sensitivity.
2. Place the π-type matching components (R1/C1/C2 and R2/C3/C4) as close to the antenna as possible.

4.1.4. Reference Design of RF Layout

For the module to be applicable to your PCB, the characteristic impedance of all RF traces should be controlled at 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

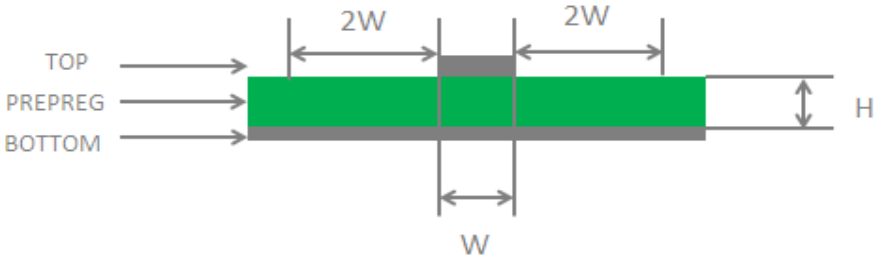


Figure 32: Reference Design of Microstrip on 2-layer PCB

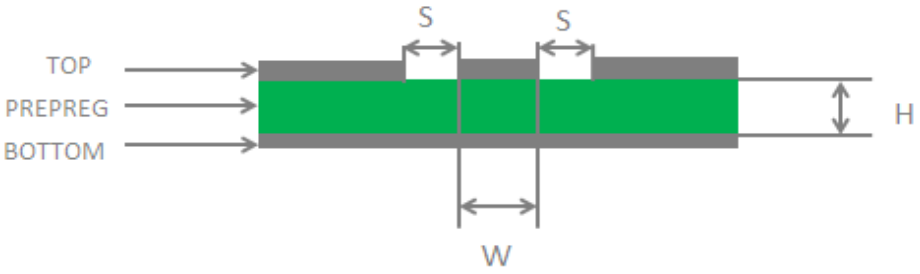


Figure 33: Reference Design of Coplanar Waveguide on 2-layer PCB

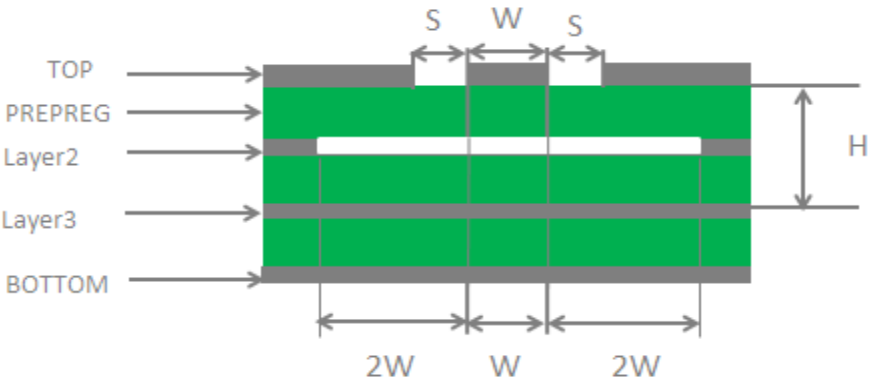


Figure 34: Reference Design of Coplanar Waveguide on 4-layer PCB (Layer 3 as Reference Ground)

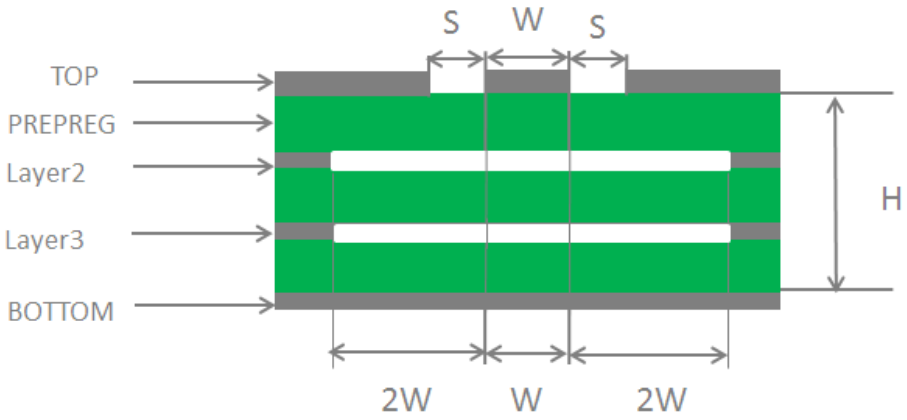


Figure 35: Reference Design of Coplanar Waveguide on 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces at 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground can help improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and parallel layout of traces on adjacent layers.

For more details about RF layout, please refer to ***document [4]***.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following table shows the requirements on main antenna and Rx-diversity antenna.

Table 29: Antenna Requirements

Type	Requirements
WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: <1 dB (WCDMA B5/B6/B8/B19, LTE B5/B8/B12/B13/B18/B19/B20/B26/B28/B29) Cable Insertion Loss: <1.5 dB (WCDMA B1/B2/B3/B4/B9, LTE B1/B2/B3/B4/B21/B25/B32/B39/B66) Cable Insertion Loss < 2 dB (LTE B7/B38/B40/B41/B30)

4.2.2. Recommended RF Connector for Antenna Installation

If an RF connector is needed for antenna connection, the U.FL-R-SMT connector provided by *Hirose* is recommended.

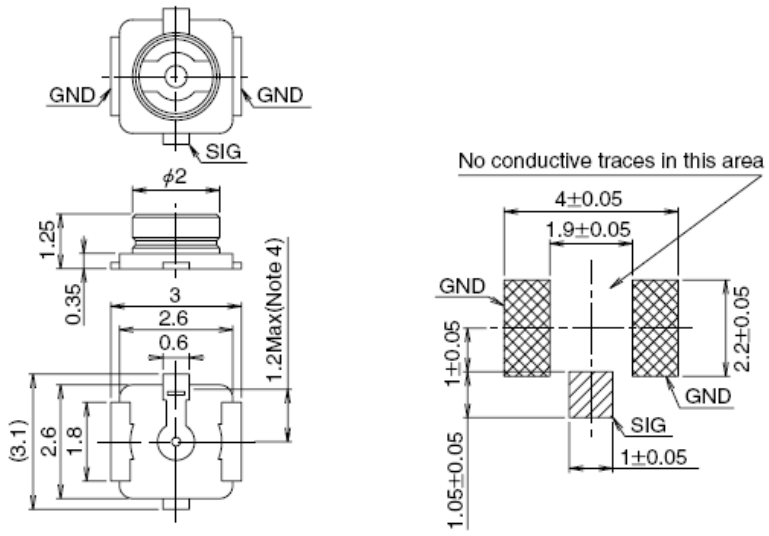


Figure 36: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP connector series listed in the following figure can be used to match the U.FL-R-SMT.

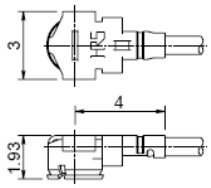
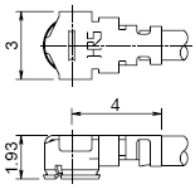
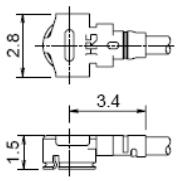
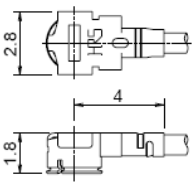
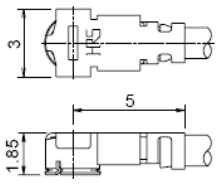
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Mechanical Features of U.FL-LP Connectors

The following figure illustrates the space factor of mated connectors.

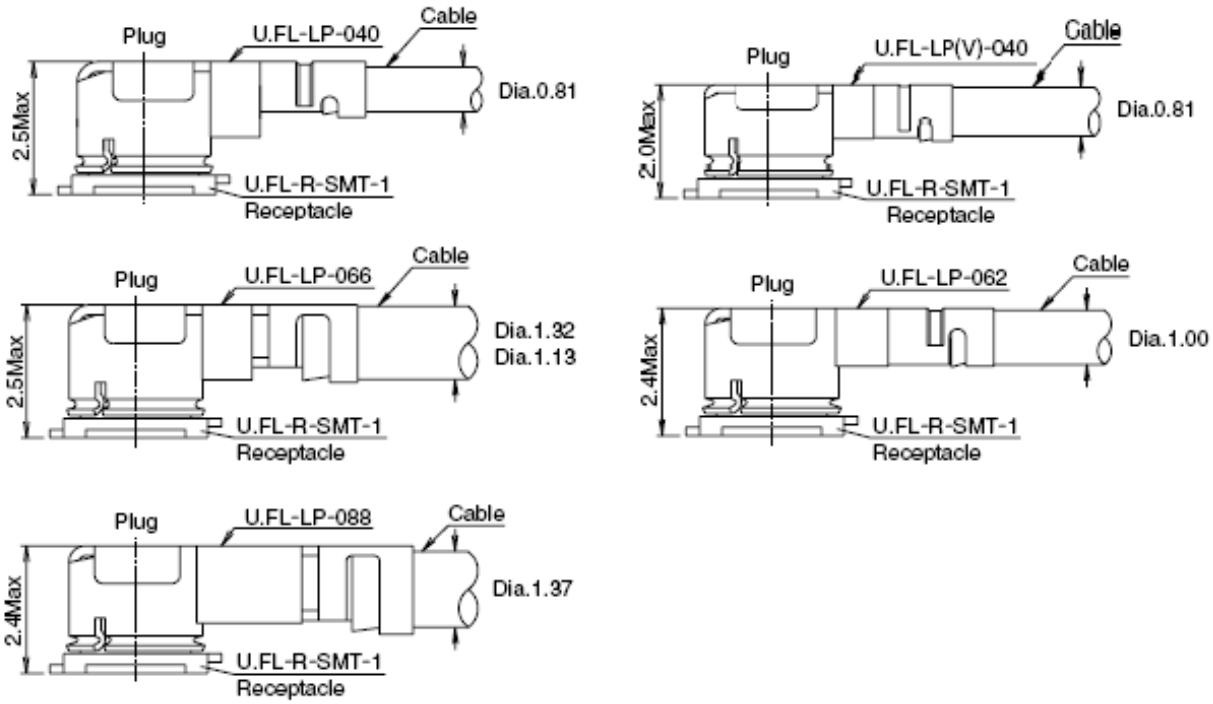


Figure 38: Form Factor of Mated Connectors (Unit: mm)

For more details, please visit https://www.hirose.com/?lang=en.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Item	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1.5	A
Peak Current of VBAT_RF	0	0.3 [1)]	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	1.4	V
Voltage at ADC1	0	1.4	V

NOTE

[1)] The current consumption is tested in 3G/4G instead of 2G environment.

5.2. Power Supply Ratings

Table 31: Module Power Supply Ratings

Item	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
USB_VBUS	USB connection detect		3.0	5.0	5.25	V

5.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 32: Operation and Storage Temperatures

Item	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-20	+25	+55	ºC
Extended Operation Range [2)]	-25		+60	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module keeps the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There won't be unrecoverable malfunctions. Nor will there be effects on the radio spectrum or harm to radio networks. Only one or more parameters like P_{out} might reduce in the value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.
3. It is not recommended to use the module without adopting a heat dissipation component. Tests are conducted at all temperature levels with heat sinks and rubber pads applied.

5.4. Current Consumption

Table 33: Module Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	10	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	2.218	mA
	WCDMA PF = 64 (USB disconnected)	4.143	mA
	WCDMA PF = 128 (USB disconnected)	3.295	mA
	WCDMA PF = 512 (USB disconnected)	2.607	mA
	LTE-FDD PF = 32 (USB disconnected)	7.171	mA
	LTE-FDD PF = 64 (USB disconnected)	4.854	mA
	LTE-FDD PF = 128 (USB disconnected)	3.643	mA
	LTE-TDD PF = 32 (USB disconnected)	7.781	mA
	LTE-TDD PF = 64 (USB disconnected)	4.984	mA
	LTE-TDD PF = 128 (USB disconnected)	3.539	mA
Idle state	WCDMA PF = 64 (USB disconnected)	29.29	mA
	WCDMA PF = 64 (USB connected)	42.99	mA
	LTE-FDD PF = 64 (USB disconnected)	29.87	mA
	LTE-FDD PF = 64 (USB connected)	43.61	mA
	LTE-TDD PF = 64 (USB disconnected)	29.89	mA
	LTE-TDD PF = 64 (USB connected)	43.89	mA
WCDMA data transfer	WCDMA B1 HSDPA CH10700 @ 22.78 dBm	571	mA
	WCDMA B1 HSUPA CH10700 @ 20.40 dBm	484	mA
	WCDMA B5 HSDPA CH4407 @ 22.64 dBm	496	mA
	WCDMA B5 HSUPA CH4407 @ 20.10 dBm	415	mA
	WCDMA B8 HSDPA CH3012 @ 22.80 dBm	544	mA

	WCDMA B8 HSUPA CH3012 @ 20.00 dBm	444	mA
LTE data transfer	LTE-FDD B1 CH300 @ 22.90 dBm	698	mA
	LTE-FDD B3 CH1575 @ 21.75 dBm	696	mA
	LTE-FDD B5 CH2525 @ 23.18 dBm	616	mA
	LTE-FDD B7 CH3100 @ 22.08 dBm	718	mA
	LTE-FDD B8 CH3625 @ 23.17 dBm	680	mA
	LTE-FDD B20 CH6300 @ 23.06 dBm	653	mA
	LTE-FDD B28 CH27435 @ 23.21 dBm	677	mA
	LTE-TDD B38 CH38000 @ 22.78 dBm	451	mA
	LTE-TDD B40 CH39150 @ 23.00 dBm	444	mA
	LTE-TDD B41 CH40740 @ 22.91 dBm	413	mA
2 × CA data transfer	LTE-FDD B1 + B1 @ 23.02 dBm	840	mA
	LTE-FDD B1 + B3 @ 22.75 dBm	868	mA
	LTE-FDD B1 + B5 @ 22.75 dBm	806	mA
	LTE-FDD B1 + B8 @ 22.74 dBm	819	mA
	LTE-FDD B1 + B20 @ 22.75 dBm	849	mA
	LTE-FDD B1 + B28 @ 22.73 dBm	851	mA
	LTE-FDD B3 + B3 @ 21.73 dBm	786	mA
	LTE-FDD B3 + B5 @ 22.71 dBm	810	mA
	LTE-FDD B3 + B7 @ 22.71 dBm	842	mA
	LTE-FDD B3 + B8 @ 22.92 dBm	808	mA
	LTE-FDD B3 + B20 @ 22.93 dBm	819	mA
	LTE-FDD B3 + B28 @ 22.92 dBm	841	mA
	LTE_FDD B5 + B7 @ 21.95 dBm	856	mA
	LTE-FDD B7 + B7 @ 22.01 dBm	876	mA
	LTE-FDD B7 + B8 @ 22.04 dBm	863	mA
	LTE-FDD B7 + B20 @ 21.98 dBm	853	mA

	LTE-FDD B7 + B28 @ 22.03 dBm	855	mA
	LTE-TDD B38 + B38 @ 21.75 dBm	490	mA
	LTE-TDD B40 + B40 @ 21.86 dBm	467	mA
	LTE-TDD B41 + B41 @ 21.79 dBm	484	mA
WCDMA voice call	WCDMA B1 CH10700 @ 22.53 dBm	545	mA
	WCDMA B5 CH4407 @ 22.66 dBm	485	mA
	WCDMA B8 CH3012 @ 22.83 dBm	532	mA

5.5. RF Output Power

The following table shows the RF output power of the module.

Table 34: RF Output Power

Frequency	Max.	Min.
WCDMA bands	24 dBm +1/-3 dB	< -50 dBm
LTE FDD bands	23 dBm ±2 Db [1)]	< -40 dBm
LTE TDD bands	23 dBm ±2 dB	< -40 dBm

NOTE

[1)] For LTE FDD Band 3, the transmitting power is 21.5 dBm ±1 dB.

5.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of the module.

Table 35: Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA B1	-109.5	/	/	-106.7
WCDMA B5	-109.5	/	/	-104.7
WCDMA B8	-109.5	/	/	-103.7
LTE-FDD B1 (10 MHz)	-97	-97	-100.5	-96.3
LTE-FDD B3 (10 MHz)	-97	-96.5	-100.5	-93.3
LTE-FDD B5 (10 MHz)	-97.5	-98	-101	-94.3
LTE-FDD B7 (10 MHz)	-95	-95.5	-97.5	-94.3
LTE-FDD B8 (10 MHz)	-97.5	-98	-101	-93.3
LTE-FDD B20 (10 MHz)	-97	-98	-101	-93.3
LTE-FDD B28 (10 MHz)	-97.5	-98	-101	-94.8
LTE-TDD B38 (10 MHz)	-97	-97	-100.5	-96.3
LTE-TDD B40 (10 MHz)	-97	-97	-100.5	-96.3
LTE-TDD B41 (10 MHz)	-96.5	-96.5	-100	-94.3

NOTE

[1)] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side to improve Rx performance.

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any

application that incorporates the module.

The following table shows the electrostatic discharge characteristics of the module.

Table 36: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.8. Thermal Consideration

To achieve better performance of the module, it is recommended to comply with the following principles out of thermal considerations:

- In your PCB design, place the module away from heating sources, especially high power components, such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted and do not cover that area with copper allowing for the adding of heatsink when necessary.
- Ensure the reference ground of the area where the module is mounted is complete, and add as many ground vias as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to particular application demands, mount the heatsink on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between heatsink and module/PCB.

Below are two reference designs of heatsink. You can choose one or both of them according to application structures.

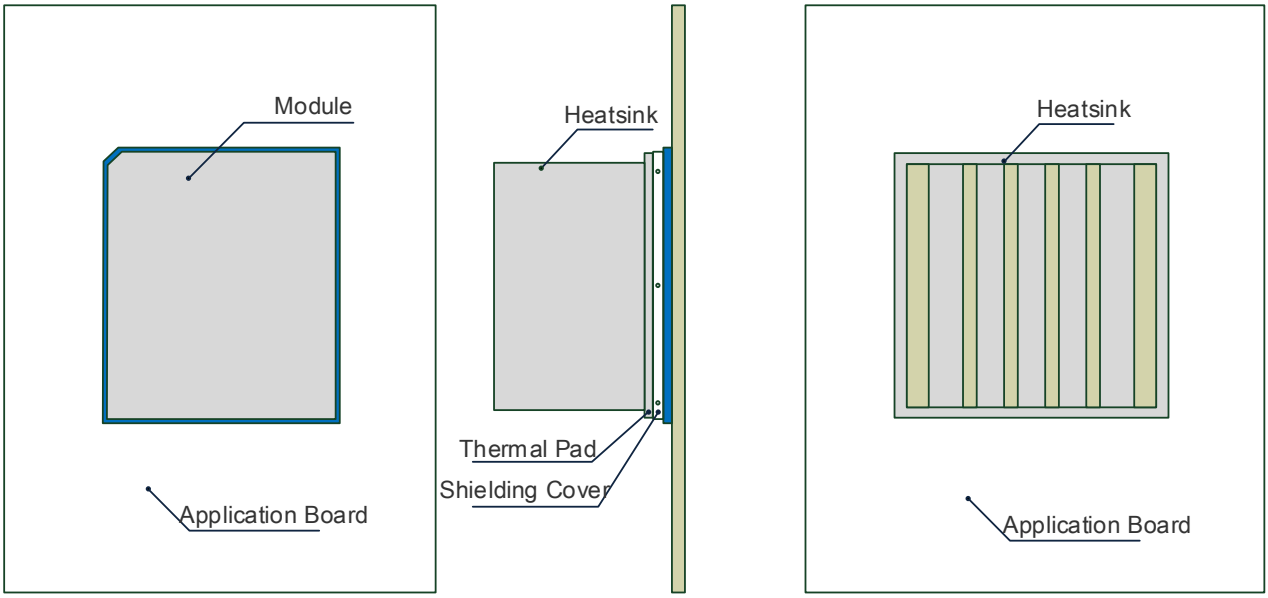


Figure 39: Reference Design of Heatsink (Heatsink at the Top of the Module)

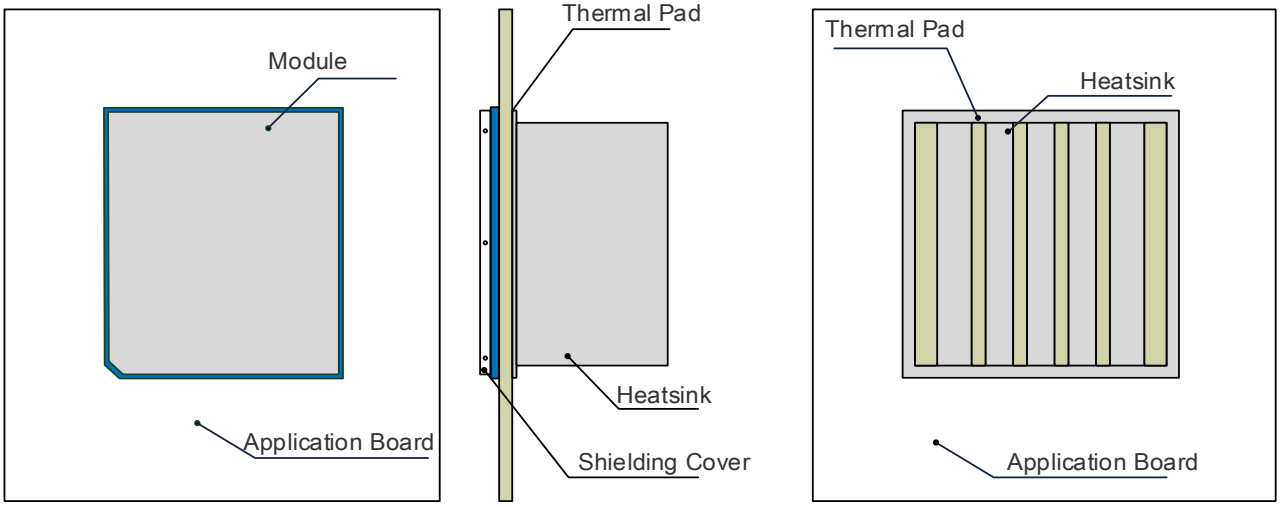


Figure 40: Reference Design of Heatsink (Heatsink at the Backside of PCB)

NOTES

1. Make sure that your PCB design provides sufficient cooling for the module: proper mounting, heatsinks, and active cooling may be required depending on the integrated application.
2. To protect components from being damaged, the thermal design should be optimized to the largest

possible extent to maintain the module's internal temperature below 105 °C. You can execute the **AT+QTEMP** command to get the module's internal temperature.

3. For more detailed guides on thermal design, please refer to ***document [5]***.

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

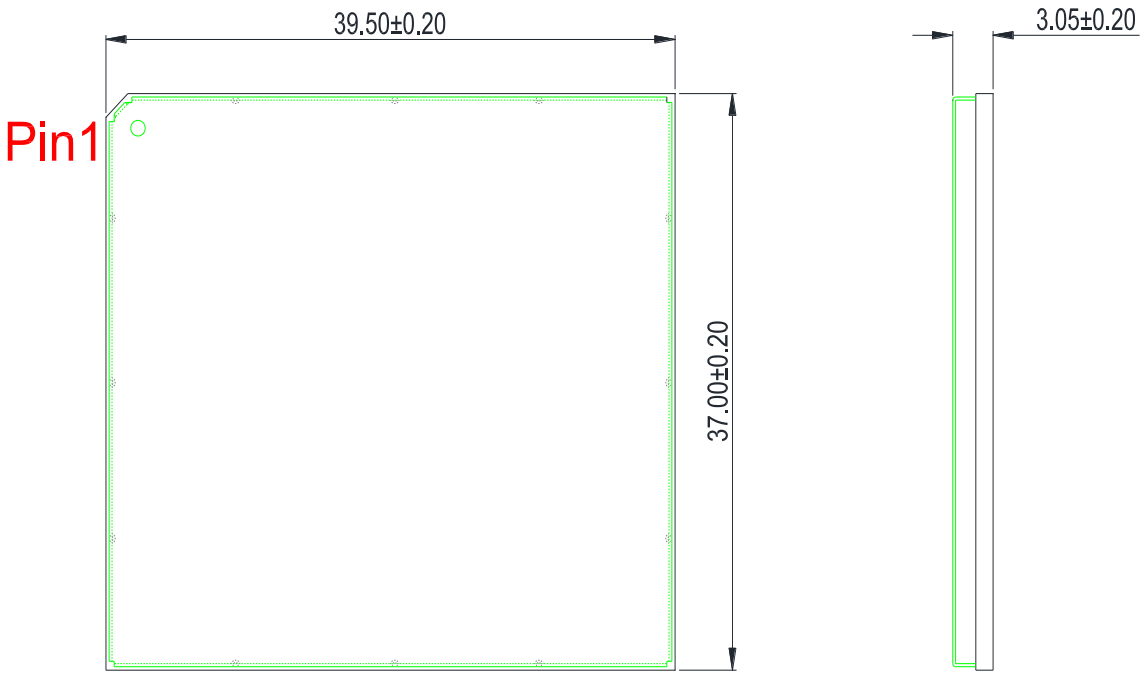


Figure 41: Top and Side Dimensions of the Module

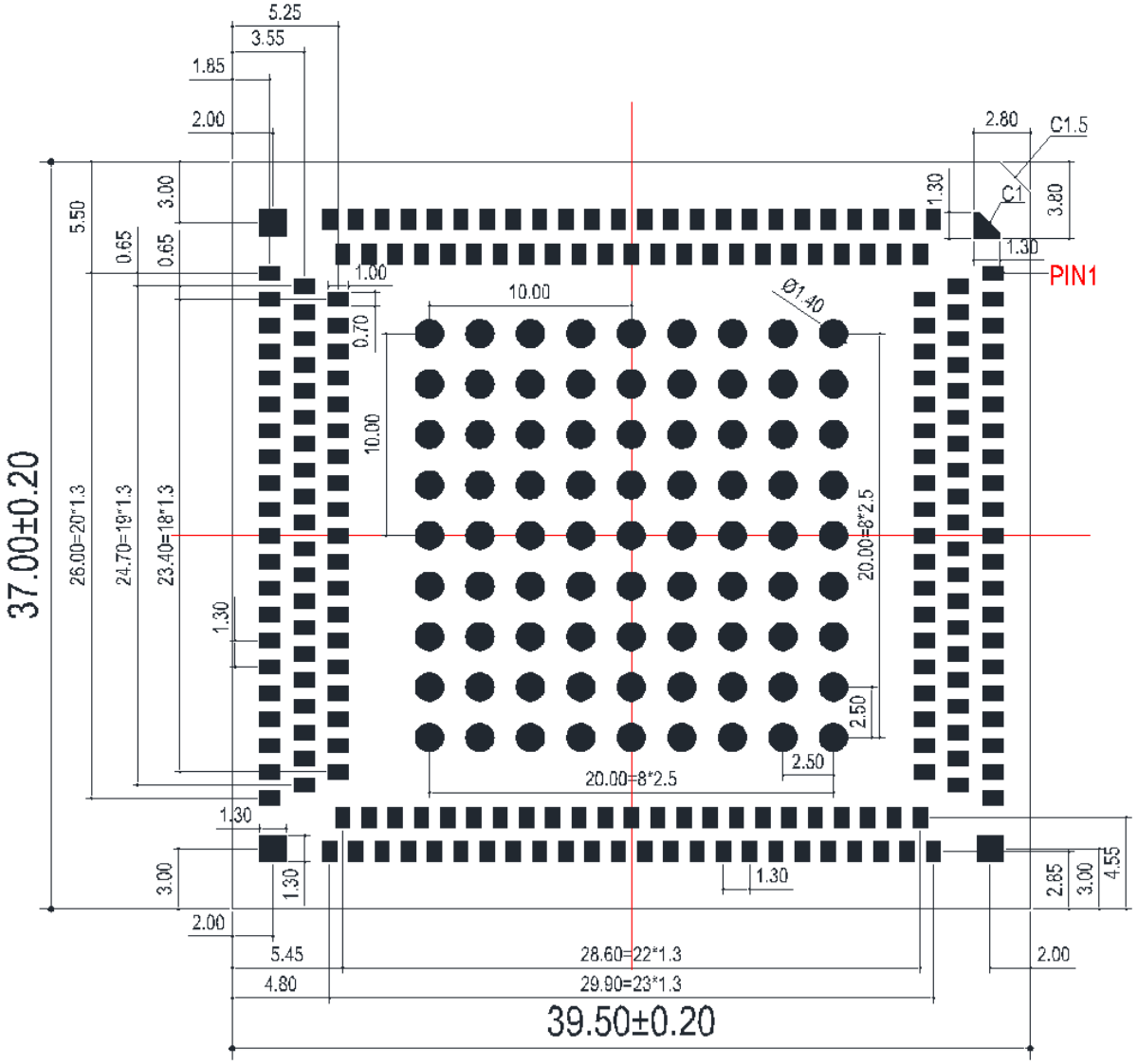


Figure 42: Bottom Dimensions (Bottom View) of the Module

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

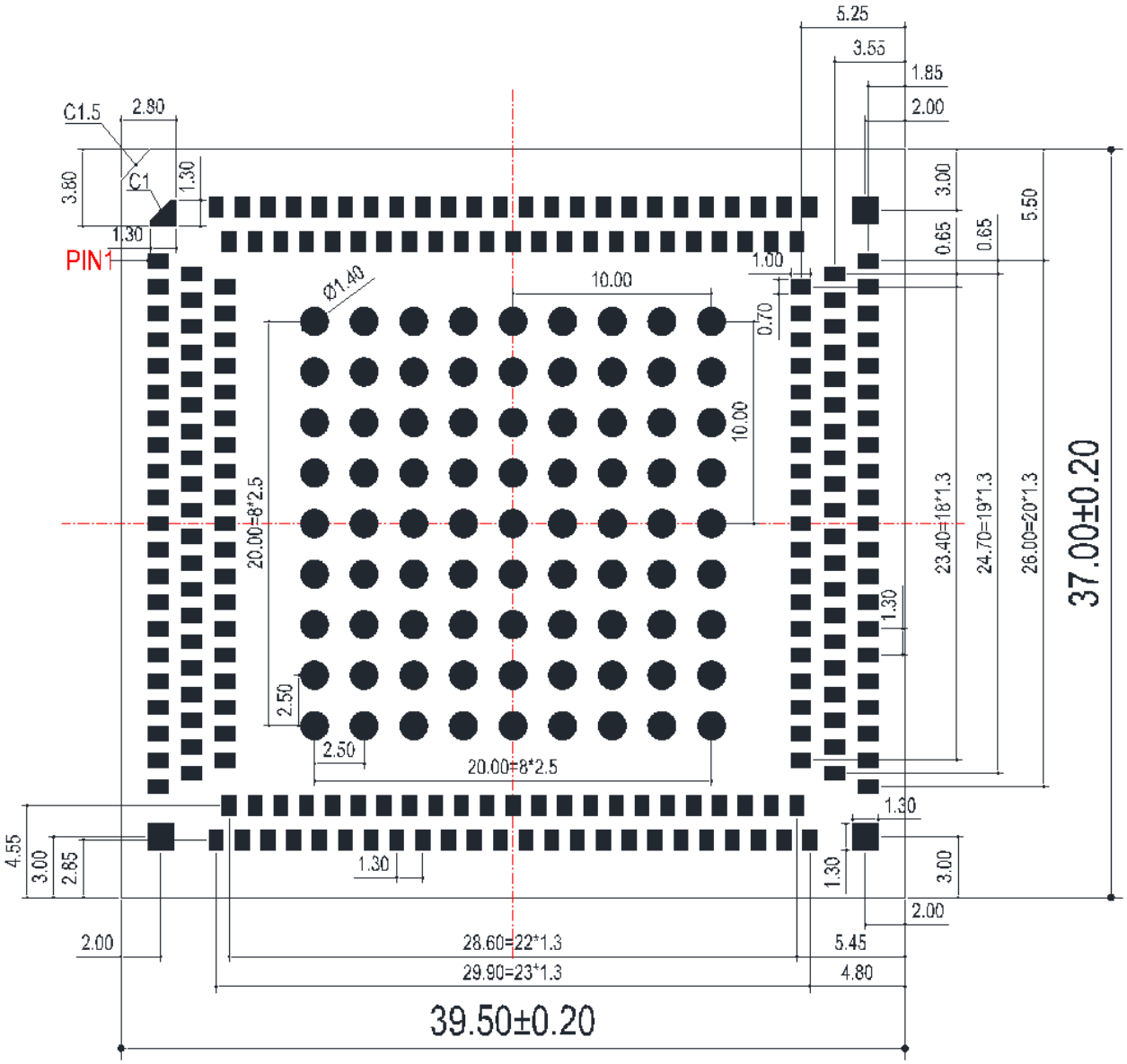


Figure 43: Recommended Footprint (Top View)

NOTE

For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.

6.3. Renderings of the Module

Figure 44: Top View of the Module

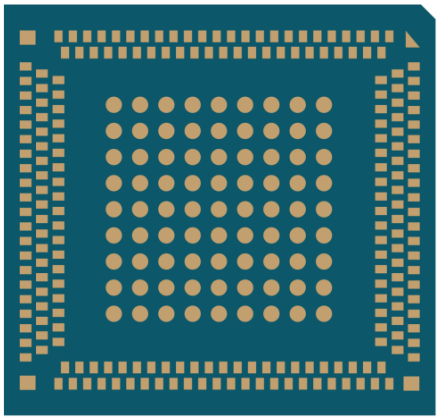


Figure 45: Bottom View of the Module

NOTE

These are renderings of EG060V-EA module. For authentic appearance, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

EG060V-EA is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, It is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, please refer to ***document [2]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

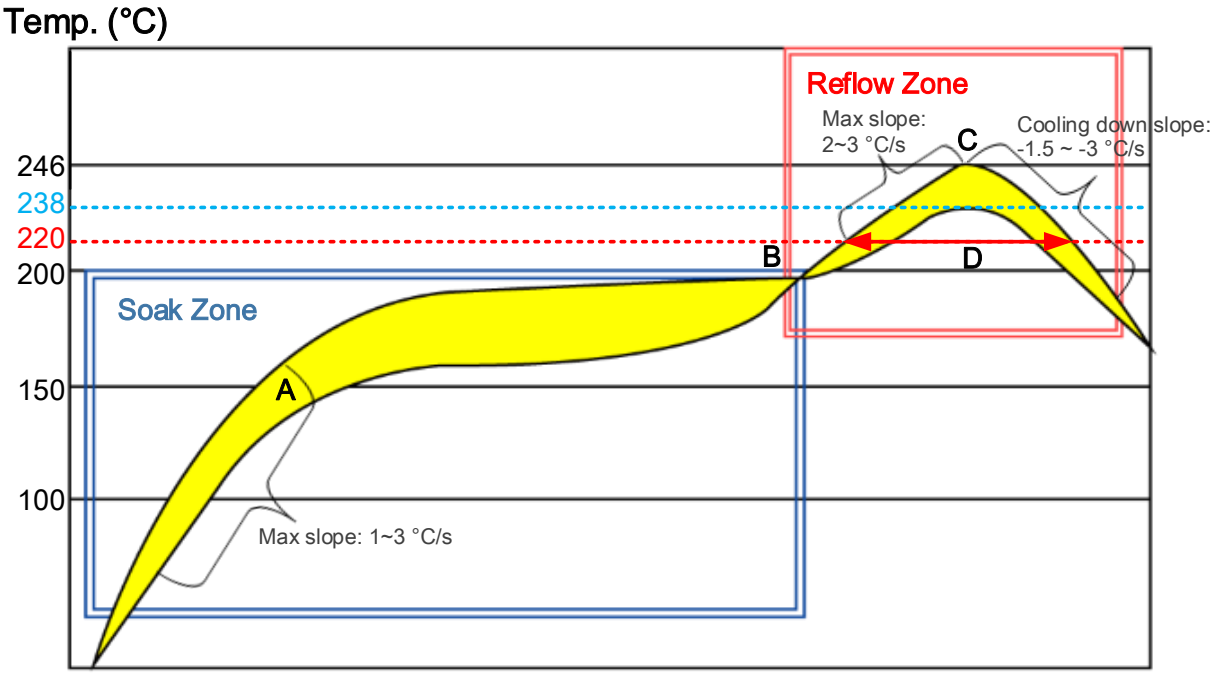


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220°C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

7.3. Packaging

EG060V-EA is packaged in tape and reel carriers. One reel is 10.56 meters long and contains 200 modules. The figures below show the packaging details, measured in mm.

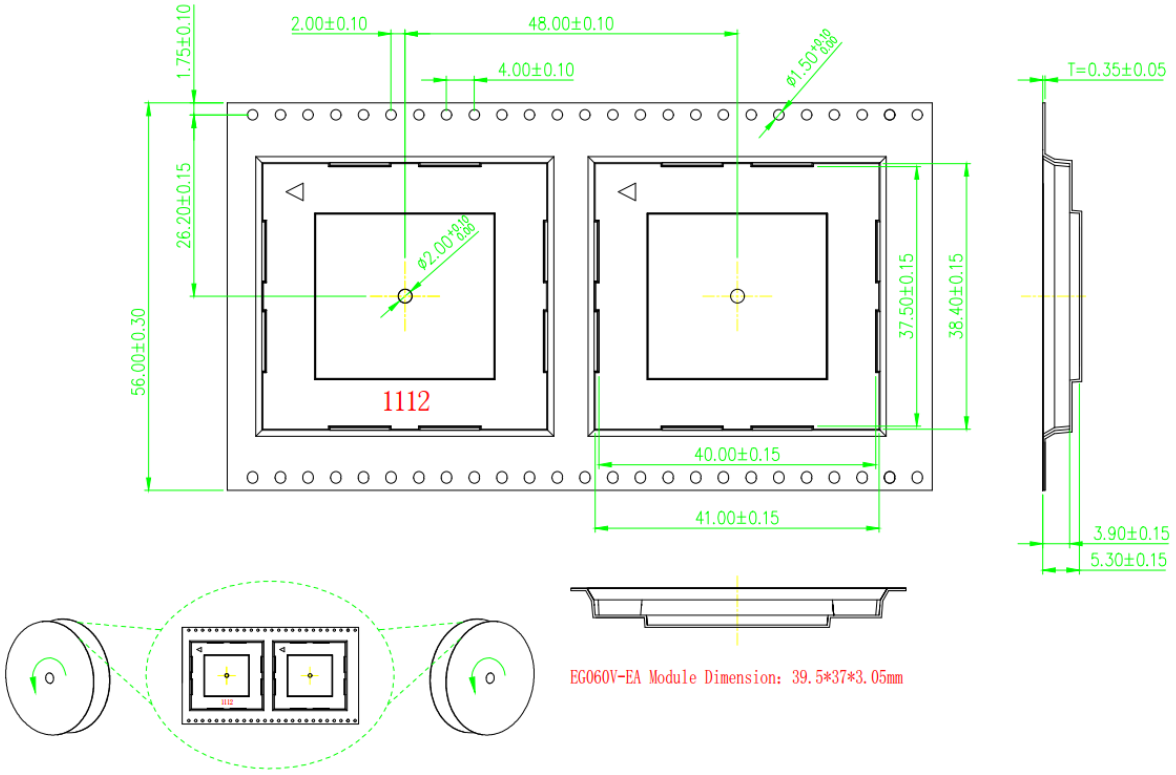


Figure 47: Tape Specifications

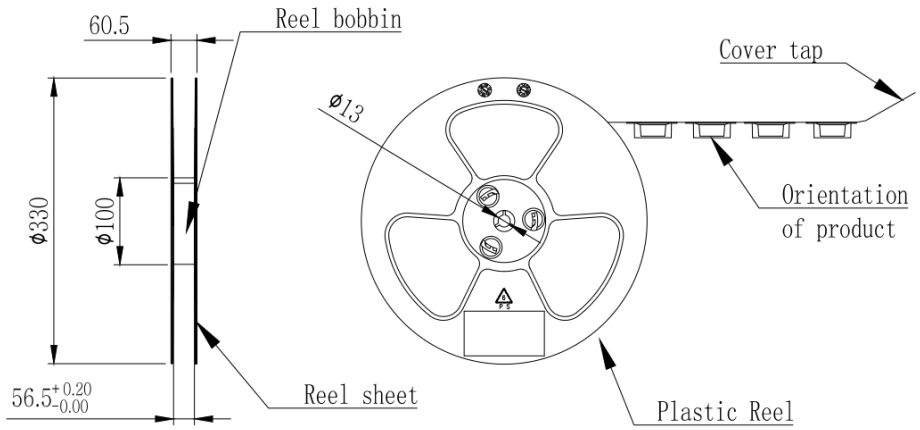


Figure 48: Reel Specifications

8 Appendix References

Table 38: Related Documents

SN	Document Name	Remark
[1]	Quectel_EG060V-EA_AT_Commands_Manual	AT Commands Manual for EG060V-EA
[2]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[3]	Quectel_EG060V-EA_Reference_Design	EG060V-EA Reference Design
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Thermal_Design_Guide	Thermal Design Guide for Quectel modules

Table 39: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DL	Downlink
DTR	Data Terminal Ready
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate

HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCC	Primary Carrier Component
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receive
SCC	Secondary Carrier Component
SIMO	Single Input Multiple Output
SMS	Short Message Service

TDD	Time Division Duplexing
Tx	Transmitting Direction
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network