SC200L Series (Dual-band Wi-Fi)

Hardware Design

Smart Module Series

Version: 1.0

Date: 2021-09-17

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.

b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.

c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.

d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Copyright © Quectel Wireless Solutions Co., Ltd. 2021. All rights reserved.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-05-26	Shihao HUANG/ Shawn HU	Creation of the document
1.0	2021-09-17	Shihao HUANG/ Shawn HU	First official release

Contents

Safety Information **3**
About the Document **4**
Contents **5**
Table Index **8**
Figure Index **10**

1 Introduction **12**
1.1. Special Mark 12

2 Product Overview **13**
2.1. Frequency Bands and Functions 13
2.2. Key Features 15
2.3. Functional Diagram 17
2.4. EVB 18

3 Application Interfaces **19**
3.1. General Description 19
3.2. Pin Assignment 20
3.3. Pin Description 21
3.4. Power Supply 32
3.4.1. Power Supply Pins 32
3.4.2. Voltage Stability Requirements 33
3.4.3. Reference Design for Power Supply 34
3.5. Turn On and Off the Module 35
3.5.1. Turn On the Module with PWRKEY 35
3.5.2. Turn Off/Restart the Module 37
3.6. Power Output 37
3.7. Battery Charging and Management 38
3.8. USB Interfaces 39
3.9. UART Interfaces 43
3.10. (U)SIM Interfaces 44
3.11. SD Card Interface 46
3.12. GPIO Interfaces 48
3.13. I2C Interfaces 50
3.14. SPI Interface 50
3.15. ADC Interface 51
3.16. LCM Interface 51
3.17. Touch Panel Interface 53
3.18. Camera Interfaces 54
3.18.1. MIPI Design considerations 57
3.19. Sensor Interfaces 58
3.20. Audio Interfaces 59
3.20.1. Reference Circuit Design for Microphone Interfaces 60

3.20.2. Reference Circuit Design for Earpiece Interface 61
3.20.3. Reference Circuit Design for Headset Interface 61
3.20.4. Reference Circuit Design for Loudspeaker Interface 62
3.20.5. Audio Signal Design Considerations 62
3.21. Emergency Download Interface 63

4 Wi-Fi and Bluetooth 64
4.1. Wi-Fi Overview 64
4.1.1. Wi-Fi Performance 64
4.2. Bluetooth Overview 66
4.2.1. Bluetooth Performance 67

5 GNSS 68
5.1. GNSS Performance 68
5.2. GNSS RF Design Guidelines 69

6 Antenna Interfaces 70
6.1. Main/Rx-diversity Antenna Interfaces 70
6.1.1. Module Operating Frequencies 70
6.1.2. Reference Circuit Design for Main and Rx-diversity Antenna Interfaces 72
6.2. Wi-Fi/Bluetooth Antenna Interface 73
6.3. GNSS Antenna Interface 74
6.3.1. Reference Circuit Design for Passive Antenna 75
6.3.2. Reference Circuit Design for Active Antenna 75
6.5. Reference Design of RF Layout 76
6.6. Antenna Installation 78
6.6.1. Antenna Requirements 78
6.6.2. Recommended RF Connector for Antenna Installation 79

7 Reliability, Radio and Electrical Characteristics 81
7.1. Absolute Maximum Ratings 81
7.2. Power Supply Ratings 81
7.3. Operating and Storage Temperatures 82
7.4. Power Consumption 82
7.5. Tx Power 90
7.6. Rx Sensitivity 93
7.7. ESD 95

8 Mechanical Information 96
8.1. Mechanical Dimensions 96
8.2. Recommended Footprint 98
8.3. Top and Bottom Views 99

9 Storage, Manufacturing and Packaging 100
9.1. Storage Conditions 100
9.2. Manufacturing and Soldering 101
9.3. Packaging Specifications 103

9.3.1. Carrier Tape 103
9.3.2. Plastic Reel 104
9.3.3. Packaging Process 104

10 Appendix References 106

Table Index

Table 1: Special Mark 12
Table 2: SC200L-CE* Frequency Bands 13
Table 3: SC200L-EU Frequency Bands 14
Table 4: SC200L-AU* Frequency Bands 14
Table 5: Key Features 15
Table 6: I/O Parameters Definition 21
Table 7: Pin Description 21
Table 8: Power Description 37
Table 9: Pin Definition of Charging Interface 38
Table 10: Pin Definition of USB1 Interface 40
Table 11: Pin Definition of USB2 Interface 41
Table 12: USB Trace Length Inside the Module 42
Table 13: Pin Definition of UART Interfaces 43
Table 14: Pin Definition of (U)SIM Interfaces 44
Table 15: Pin Definition of SD Card Interface 46
Table 16: SD Card Signal Trace Length Inside the Module 47
Table 17: Pin Definition of GPIO Interfaces 48
Table 18: Pin Definition of I2C Interfaces 50
Table 19: Pin Definition of SPI Interface 50
Table 20: Pin Definition of ADC Interface 51
Table 21: Pin Definition of LCM Interface 51
Table 22: Pin Definition of Touch Panel Interface 53
Table 23: Pin Definition of Camera Interfaces 55
Table 24: MIPI Trace Length Inside the Module 57
Table 25: Pin Definition of Sensor Interfaces 58
Table 26: Pin Definition of Audio Interfaces 59
Table 27: Wi-Fi Transmitting Performance 64
Table 28: Wi-Fi Receiving Performance 65
Table 29: Bluetooth Data Rate and Versions 67
Table 30: Bluetooth Transmitting and Receiving Performance 67
Table 31: GNSS Performance 68
Table 32: Pin Definition of Main/Rx-diversity Antenna Interfaces 70
Table 33: SC200L-CE* Module Operating Frequencies 70
Table 34: SC200L-EU Module Operating Frequencies 71
Table 35: SC200L-AU* Module Operating Frequencies 72
Table 36: Pin Definition of Wi-Fi/Bluetooth Antenna Interface 73
Table 37: Wi-Fi/Bluetooth Frequency 73
Table 38: Pin Definition of GNSS Antenna 74
Table 39: GNSS Frequencies 74
Table 40: Antenna Requirements 78
Table 41: Absolute Maximum Ratings 81

Table 42: Power Supply Ratings 81
Table 43: Operating and Storage Temperatures 82
Table 44: SC200L-CE* Power Consumption 82
Table 45: SC200L-EU Power Consumption 84
Table 46: SC200L-AU* Power Consumption 87
Table 47: SC200L-CE* RF Output Power 90
Table 48: SC200L-EU RF Output Power 91
Table 49: SC200L-AU* RF Output Power 92
Table 50: SC200L-CE* RF Receiving Sensitivity 93
Table 51: SC200L-EU RF Receiving Sensitivity 94
Table 52: SC200L-AU* RF Receiving Sensitivity 94
Table 53: ESD Characteristics (Temperature: 25 °C, Humidity: 45 %) 95
Table 54: Recommended Thermal Profile Parameters 102
Table 55: Carrier Tape Dimension Table (Unit: mm) 103
Table 56: Plastic Reel Dimension Table (Unit: mm) 104
Table 57: Related Documents 106
Table 58: Terms and Abbreviations 106

Figure Index

Figure 1: Functional Diagram 18
Figure 2: Pin Assignment (Perspective View) 20
Figure 3: Voltage Drop Sample 33
Figure 4: Star Structure of Power Supply 34
Figure 5: Reference Circuit of Power Supply 34
Figure 6: Turn On the Module Using Driving Circuit 35
Figure 7: Turn On the Module Using Keystroke 35
Figure 8: Power-Up Timing 36
Figure 9: Restart Timing 37
Figure 10: Reference Design for Battery Charging Circuit 39
Figure 11: Reference Design for USB1 Interface 40
Figure 12: Reference Design for USB1 Power Supply 41
Figure 13: Reference Design for USB2 Interface 41
Figure 14: Reference Design for USB2 Power Supply 42
Figure 15: Reference Circuit with Level Translator Chip (for UART0) 43
Figure 16: RS-232 Level Match Circuit (for UART0) 44
Figure 17: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector 45
Figure 18: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector 45
Figure 19: Reference Circuit for SD Card Interface 47
Figure 20: Reference Circuit Design for LCM Interface 52
Figure 21: Reference Design of LCM External Backlight Driving Circuit 53
Figure 22: Reference Circuit Design for Touch Panel Interface 54
Figure 23: Reference Circuit Design for Two-Camera Applications 56
Figure 24: Reference Design for ECM Microphone 60
Figure 25: Reference Design for MEMS Microphone 60
Figure 26: Reference Circuit Design for Earpiece Interface 61
Figure 27: Reference Circuit Design for Headset Interface 61
Figure 28: Reference Circuit Design for Loudspeaker Interface 62
Figure 29: Reference Circuit Design for Emergency Download Interface 63
Figure 30: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces 73
Figure 31: Reference Circuit Design for Wi-Fi/Bluetooth Antenna Interface 74
Figure 32: Reference Circuit Design for GNSS Passive Antenna 75
Figure 33: Reference Circuit Design for GNSS Active Antenna 75
Figure 34: Microstrip Line Design on a 2-layer PCB 76
Figure 35: Coplanar Waveguide Line Design on a 2-layer PCB 76
Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground) 77
Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground) 77
Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm) 79
Figure 39: Mechanicals of U.FL-LP Connectors 79
Figure 40: Space Factor of Mated Connector (Unit: mm) 80
Figure 41: Module Top and Side Dimensions 96

Figure 42: Module Bottom Dimensions (Bottom View) 97
Figure 43: Recommended Footprint (Top View) 98
Figure 44: Top and Bottom Views 99
Figure 45: Recommended Reflow Soldering Thermal Profile 101
Figure 46: Carrier Tape Dimension Drawing 103
Figure 47: Plastic Reel Dimension Drawing 104
Figure 48: Packaging Process 105

1 Introduction

This document, describing SC200L series (Dual-band Wi-Fi) module and its air and hardware interfaces connected to your applications, informs you of the interface specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

SC200L series (Dual-band Wi-Fi) is a series of smart LTE module based on Android operating system, and provides industrial grade performance. Its general features are listed below:

- Supports LTE-FDD, LTE-TDD, HSDPA, HSUPA, WCDMA, EDGE, GSM and GPRS coverage.
- Supports short-range wireless communication through Wi-Fi 802.11a/b/g/n/ac and Bluetooth 5.0.
- Integrates GPS/GLONASS/BeiDou satellite positioning systems.
- Supports multiple audio and video codecs.
- Built-in high-performance Mail-T820 graphics processing unit.
- Provides multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

SC200L series (Dual-band Wi-Fi) is available in three variants: SC200L-CE*, SC200L-EU, and SC200L-AU*.

The module supports multiple standards and multiple frequency bands. The corresponding standards and frequency bands are as follows:

Table 2: SC200L-CE* Frequency Bands

Mode	Frequency bands
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41(140 MHz)
WCDMA	B1/B8
GSM	900/1800 MHz
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz
Bluetooth 5.0	2402–2480 MHz

GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz

Table 3: SC200L-EU Frequency Bands

Mode	Frequency bands
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41(200 MHz)
WCDMA	B1/B5/B8
GSM	900/1800 MHz
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz
Bluetooth 5.0	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz

Table 4: SC200L-AU* Frequency Bands

Mode	Frequency bands
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B28
LTE-TDD	B38
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900 MHz
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz
Bluetooth 5.0	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz

The module is an SMD module with a total of 274 pins, including 146 LCC pins and 128 LGA pins. The size is only 40.5 mm × 40.5 mm × 2.85 mm, which can be embedded in various M2M product applications through pads. It is very suitable for the development of mobile devices such as POS machines, in-vehicle computers, multimedia terminals, smart homes, and IoT terminals.

2.2. Key Features

Table 5: Key Features

Features	Details
CPU	Quad-core ARM Cortex-A53 CPU @ 1.4 GHz 32 KB L1 I-cache, 32 KB L1 D-cache, 256 KB L2 cache
GPU	Mali-T820 MP1 GPU, working at 680 MHz
Memory	● 8 GB eMMC + 1 GB LPDDR3 (default) ● 16 GB eMMC + 2 GB LPDDR3 (optional)
System	Android 10.0
Power	VBAT power supply rang: 3.50–4.20 V Typical supply voltage: 3.80 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for GSM850 Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class 1 (30 dBm ±2 dB) for PCS1900 Class E2 (27 dBm ±3 dB) for GSM850 8-PSK Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK Class 3 (23 dBm ±2 dB) for WCDMA bands Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Supports 3GPP Rel-10 Cat 4 FDD and TDD Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● FDD: Max. 150 Mbps (DL)/ Max. 50 Mbps (UL) ● TDD: Max. 130 Mbps (DL)/ Max. 30 Mbps (UL)
UMTS Features	Supports 3GPP Rel-9 HSDPA/HSUPA/WCDMA Supports QPSK, 16QAM and 64QAM modulation ● HSDPA: Max. 21 Mbps ● HSUPA: Max. 11 Mbps ● WCDMA: Max. 384 kbps (DL)/ Max. 384 kbps (UL)

GSM Features	**R99** **GPRS** Supports GPRS multi-slot level 33 (default 33) Coding format: CS-1, CS-2, CS-3 and CS-4 Max. 107 kbps (DL)/ Max. 85.6 kbps (UL) **EDGE** Supports EDGE multi-slot level 33 (default 33) Supports GMSK and 8-PSK modulation and coding methods Downlink coding format: MCS 1–9 Uplink coding format: MCS 1–9 Max. 296 kbps (DL)/ Max. 236.8 kbps (UL)
WLAN Features	Supports AP mode and STA mode ● 2.4 GHz, supports 802.11b/g/n, up to 150 Mbps ● 5 GHz, supports 802.11a/n/ac, up to 433 Mbps
Bluetooth Features	Supports Bluetooth 5.0 Supports Bluetooth Classic and BLE
GNSS	GPS + GLONASS or GPS + BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS SMS cell broadcast
LCM Interface	Supports 1 group of 4-lane MIPI_DSI, up to 1.5 Gbps/lane Supports up to HD+ (1440 × 720) @ 60 fps
Camera Interfaces	Supports 2 groups of MIPI_CSI, up to 1.5 Gbps/lane ● Front camera: 1-lane MIPI, which can support up to 2 MP camera ● Rear camera: 2-lane MIPI, which can support up to 8 MP camera
Video codec	Video codec: encoding + decoding: 1080P @ 30 fps + 1080P @ 30 fps Wi-Fi video: encoding up to 720P @ 30 fps, decoding up to 1080P @ 30 fps
Audio Interfaces	**Audio input** 3 analog microphone inputs, external bias voltage circuit is needed **Audio output** ● Class AB stereo headphone output ● Class AB differential earpiece output ● Class D differential speaker amplifier output
Audio codec	GSM-FR, GSM-EFR, GSM-HR, AMR, AMR-NB, AMR-WB, EVS-NB, EVS-WB, EVS-SWB, MP3, AAC, AAC+, PCM
USB Interfaces	Supports 2 USB interfaces which comply with USB 2.0 specification ● USB1: – Supports USB OTG, but does not support USB hub, up to 480 Mbps – Used for AT command transmission, data transmission, software debugging and firmware upgrade ● USB2 – Supports USB host mode only, supports USB hub, up to 100 Mbps

UART Interfaces	2 UART interfaces: ● UART0: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 3.25 Mbps ● Debug UART: 2-wire UART interface, used for debugging by default
SD Card Interface	Supports SD 3.0 Supports 1.8 V or 3.0 V SD card Supports SD card hot-plug
(U)SIM Interfaces	2 (U)SIM interfaces Supports USIM/SIM card: 1.80 V or 2.95 V Supports Dual Card Dual Standby by default
I2C Interfaces	4 I2C interfaces Used for peripherals such as touch screen, camera, sensor, etc.
SPI Interface	1 SPI interface multiplexed from GPIO interfaces Used for fingerprint recognition or other peripherals
ADC Interface	1 general-purpose ADC interface Supports up to 12-bit resolution
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna, Wi-Fi/Bluetooth antenna interfaces
Physical Characteristics	Size: (40.5 ±0.15) mm × (40.5 ±0.15) mm × (2.85 ±0.2) mm Package: LCC + LGA Weight: Approx. 10.0 g
Temperature Range	● Operating temperature range: -30 °C to +75 °C [1] ● Storage temperature range: -40 °C to +90 °C
Software Upgrade	Via USB interface or OTA
RoHS	All hardware components are fully compliant with EU RoHS standards

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- RF part
- Baseband part
- LPDDR3 + eMMC memory
- Peripheral interfaces
  -- USB interfaces
  -- (U)SIM interfaces
  -- UART interfaces

[1] Within the operating temperature range, the module is 3GPP compliant.

-- SD card interface
-- I2C interfaces
-- ADC interface
-- LCM (MIPI) interface
-- TP (Touch Panel) interface
-- Camera (MIPI) interfaces
-- Audio interfaces

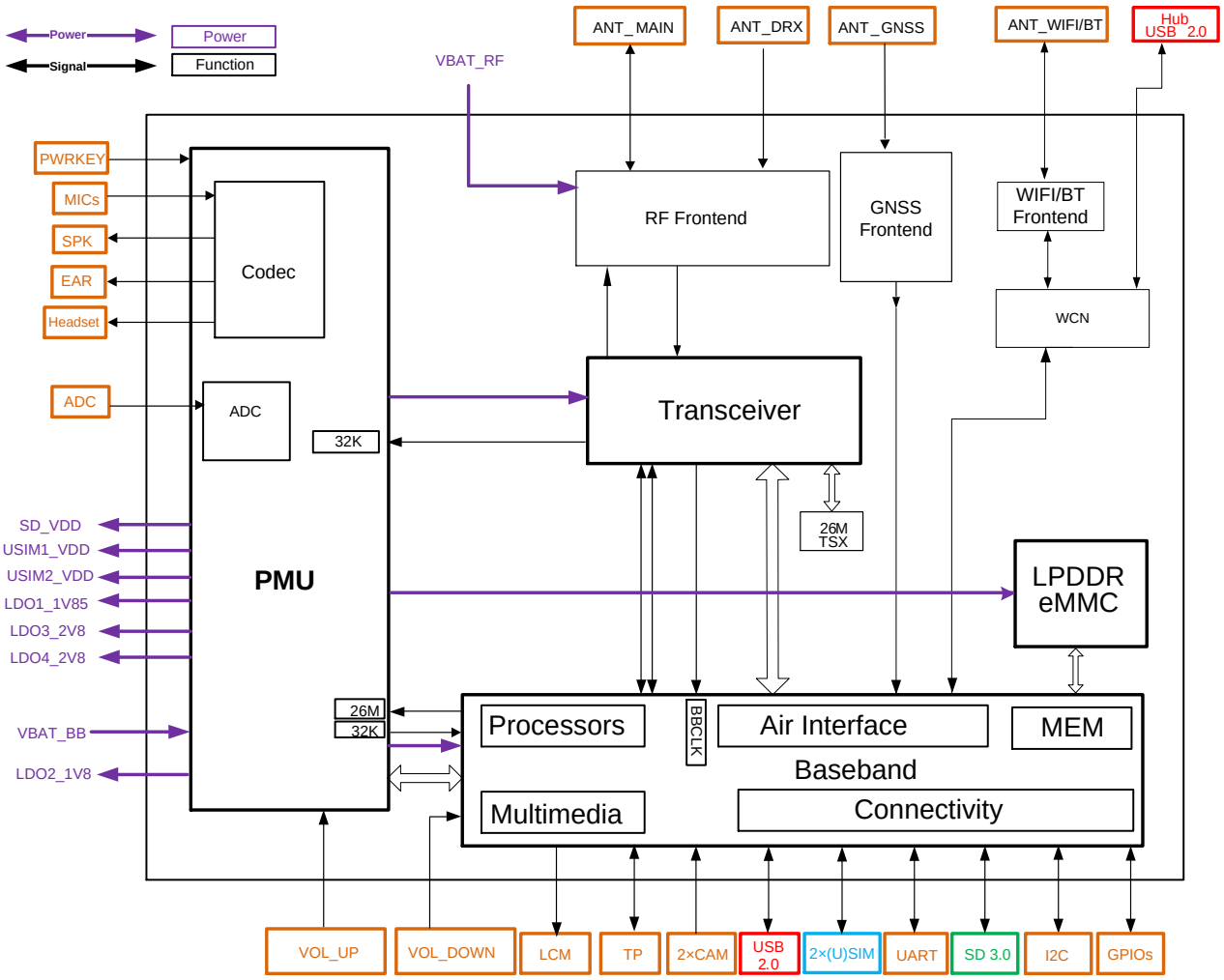


Figure 1: Functional Diagram

2.4. EVB

To help you design and test applications with the module, Quectel supplies an evaluation kit, which includes an evaluation board, a USB to RS-232 converter cable, a USB data cable, an earphone, antennas, etc. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- USB interfaces
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- SPI interface
- ADC interface
- LCM interface
- Touch panel interface
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

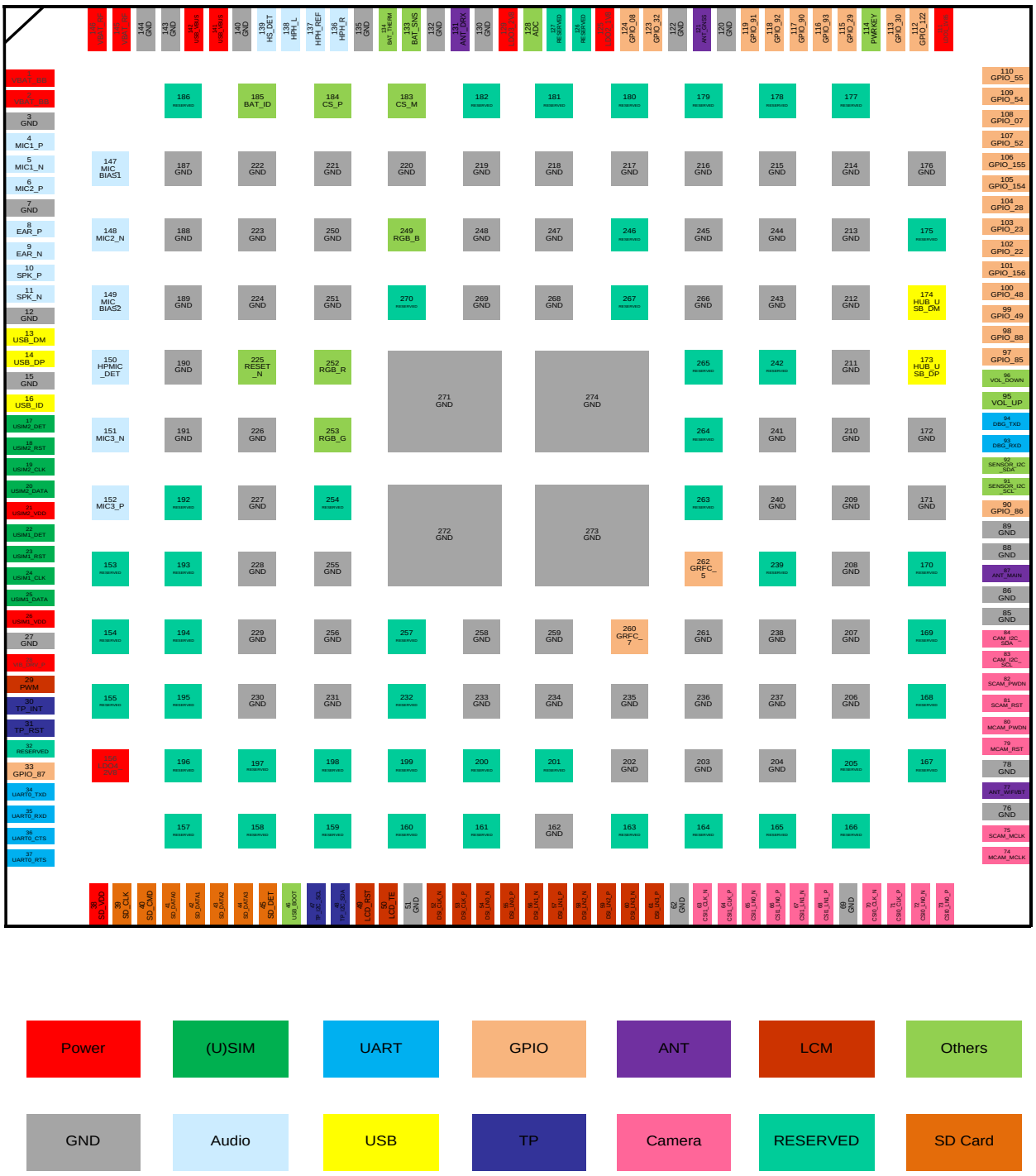


Figure 2: Pin Assignment (Perspective View)

3.3. Pin Description

Table 6: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	1, 2	PIO	Power supply for module's baseband part	Vmax = 4.20 V Vmin = 3.50 V Vnom = 3.80 V	Provide them with sufficient current of at least 3 A. It is suggested to add a TVS diode for surge protection.
VBAT_RF	145, 146	PI	Power supply for module's RF part.	Vmax = 4.20 V Vmin = 3.50 V Vnom = 3.80 V	
LDO1_1V85	111	PO	1.85 V output power supply	Vnom = 1.85 V $I_O$max = 100 mA	Power supply for external GPIO's pull-up and level shift circuits.
LDO2_1V8	125	PO	1.8 V output power supply	Vnom = 1.80 V $I_O$max = 200 mA	I/O power supply for sensor, camera, and other external devices.

LDO4_2V8	156	PO	2.80 V output power supply	Vnom = 2.80 V $I_O$max = 200 mA	Power supply for LCD, TP and sensor. If it is used, connect an external capacitor to this pin in parallel. See ***document [2]*** for details. If not used, keep it open.
LDO3_2V8	129	PO	2.80 V output power supply	Vnom = 2.80 V $I_O$max = 150 mA	Power supply for camera AVDD and AFVDD. If it is used, connect an external capacitor to this pin in parallel. See ***document [2]*** for details. If not used, keep it open.

GND

Pin Name	Pin No.
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 162, 171, 172, 176, 187, 188, 189, 190, 191, 202, 203, 204, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 226, 227, 228, 229, 230, 231, 233, 234, 235, 236, 237, 238, 240, 241, 243, 244, 245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271, 272, 273, 274

Audio Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC1_P	4	AI	Microphone input for channel 1 (+)		
MIC1_N	5	AI	Microphone input for channel 1 (-)		
MIC2_P	6	AI	Microphone input for headset (+)		
MIC2_N	148	AI	Microphone input for headset (-)		
EAR_P	8	AO	Earpiece output (+)		
EAR_N	9	AO	Earpiece output (-)		
SPK_P	10	AO	Speaker output (+)		

SPK_N	11	AO	Speaker output (-)		
HPH_R	136	AO	Headphone right channel output		
HPH_REF	137	AO	Headphone reference ground		If it is not used, connect it to ground.
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset insertion detect		High level by default.
HPMIC_DET	150	AI	Headphone microphone detect		
MIC_BIAS1	147	PO	Microphone bias voltage 1	Vmin = 2.20 V Vmax = 3.00 V Vnom = 2.50 V	
MIC3_P	152	AI	Microphone input for channel 2 (+)		
MIC3_N	151	AI	Microphone input for channel 2 (-)		
MIC_BIAS2	149	PO	Microphone bias voltage 2	Vmin = 2.20 V Vmax = 3.00 V Vnom = 2.80 V	
USB1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	141, 142	PI	Charging power input; USB 5 V power input; USB/adaptor insertion detect	Vmax = 9.20 V Vmin = 4.50 V Vnom = 5.00 V	
USB_DM	13	AIO	USB differential data bus (-)		USB 2.0 standard compliant. 90 Ω differential impedance. Supports USB OTG mode, but does not support USB hub.
USB_DP	14	AIO	USB differential data bus (+)		
USB_ID	16	DI	USB ID detection		High level by default. If not used, keep it open.
USB2 Interface					

HUB_USB_DP	173	AIO	USB differential data bus (+)	USB 2.0 standard compliant. 90 Ω differential impedance. Supports USB host mode only and supports USB hub.
HUB_USB_DM	174	AIO	USB differential data bus (-)	
(U)SIM Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	V_{IL}max=0.48 V V_{IH}min=1.39 V	This function is enabled by default. Active low. If it is not used, keep it open.
USIM2_RST	18	DO	(U)SIM2 card reset	V_{OL}max = 0.1 × USIM2_VDD V_{OH}min = 0.9 × USIM2_VDD	
USIM2_CLK	19	DO	(U)SIM2 card clock	V_{OL}max = 0.1 × USIM2_VDD V_{OH}min = 0.9 × USIM2_VDD	
USIM2_DATA	20	DIO	(U)SIM2 card data	V_{IL}max = 0.3 × USIM2_VDD V_{IH}min = 0.7 × USIM2_VDD V_{OL}max = 0.1 × USIM2_VDD V_{OH}min = 0.9 × USIM2_VDD	
USIM2_VDD	21	PO	(U)SIM2 card power supply	**1.80 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.90 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	This function is enabled by default. Active low. If it is not used, keep it open.

USIM1_RST	23	DO	(U)SIM1 card reset	V_{OL}max = 0.1 × USIM1_VDD V_{OH}min = 0.9 × USIM1_VDD	
USIM1_CLK	24	DO	(U)SIM1 card clock	V_{OL}max = 0.1 × USIM1_VDD V_{OH}min = 0.9 × USIM1_VDD	
USIM1_DATA	25	DIO	(U)SIM1 card data	V_{IL}max = 0.3 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.1 × USIM1_VDD V_{OH}min = 0.9 × USIM1_VDD	
USIM1_VDD	26	PO	(U)SIM1 card power supply	**1.80 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.90 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART0_TXD	34	DO	UART0 transmit	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	1.85 V power domain. If not used, keep these pins open.
UART0_RXD	35	DI	UART0 receive	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	
UART0_CTS	36	DI	DCE clear to send	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	
UART0_RTS	37	DO	DCE request to send	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
DBG_RXD	93	DI	Debug UART receive	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	
DBG_TXD	94	DO	Debug UART transmit	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SD_VDD	38	PO	SD card power supply	Vnom = 3.00 V $I_O$max = 400 mA	If a large-capacity T-Flash card is to be connected, it is recommended to add an LDO which can supply 1 A current.
SD_CLK	39	DO	SD card clock	**1.8 V SD card:** V_{OL}max = 0.19 V V_{OH}min = 1.58 V **3.0 V SD card:** V_{OL}max = 0.31 V V_{OH}min = 2.61 V	50 Ω characteristic impedance.
SD_CMD	40	DIO	SD card command	**1.8 V SD card:** V_{IL}max = 0.53 V V_{IH}min = 1.30 V V_{OL}max = 0.19 V V_{OH}min = 1.58 V **3.0 V SD card:** V_{IL}max = 0.87 V V_{IH}min = 2.17 V V_{OL}max = 0.31 V V_{OH}min = 2.61 V	
SD_DATA0	41	DIO	SDIO data bits		
SD_DATA1	42	DIO			
SD_DATA2	43	DIO			
SD_DATA3	44	DIO			
SD_DET	45	DI	SD card hot-plug detect	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	Active low.
Touch Panel (TP) Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_INT	30	DI	TP interrupt	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	1.85 V power domain.
TP_RST	31	DO	TP reset	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	1.85 V power domain. Active low.
TP_I2C_SCL	47	OD	TP I2C clock		1.85 V power domain. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM	29	DO	PWM output	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	Adjusts backlight brightness. 1.85 V power domain.

LCD_RST	49	DO	LCD reset	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	1.85 V power domain.
LCD_TE	50	DI	LCD tearing effect	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	1.85 V power domain.
DSI_CLK_N	52	AO	MIPI DSI clock (-)		
DSI_CLK_P	53	AO	MIPI DSI clock (+)		
DSI_LN0_N	54	AO	MIPI DSI data 0 (-)		
DSI_LN0_P	55	AO	MIPI DSI data 0 (+)		
DSI_LN1_N	56	AO	MIPI DSI data 1 (-)		
DSI_LN1_P	57	AO	MIPI DSI data 1 (+)		
DSI_LN2_N	58	AO	MIPI DSI data 2 (-)		
DSI_LN2_P	59	AO	MIPI DSI data 2 (+)		
DSI_LN3_N	60	AO	MIPI DSI data 3 (-)		
DSI_LN3_P	61	AO	MIPI DSI data 3 (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI1_CLK_N	63	AI	MIPI clock of rear camera (-)		
CSI1_CLK_P	64	AI	MIPI clock of rear camera (+)		
CSI1_LN0_N	65	AI	MIPI lane 0 data of rear camera (-)		
CSI1_LN0_P	66	AI	MIPI lane 0 data of rear camera (+)		
CSI1_LN1_N	67	AI	MIPI lane 1 data of rear camera (-)		
CSI1_LN1_P	68	AI	MIPI lane 1 data of rear camera (-)		

CSI0_CLK_N	70	AI	MIPI clock of front camera (-)		
CSI0_CLK_P	71	AI	MIPI clock of front camera (+)		
CSI0_LN0_N	72	AI	MIPI lane 0 data of front camera (-)		
CSI0_LN0_P	73	AI	MIPI lane 0 data of front camera (+)		
MCAM_MCLK	74	DO	Master clock of rear camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	1.85 V power domain.
SCAM_MCLK	75	DO	Master clock of front camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
MCAM_RST	79	DO	Reset of rear camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
MCAM_PWDN	80	DO	Power down of rear camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
SCAM_RST	81	DO	Reset of front camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
SCAM_PWDN	82	DO	Power down of front camera	V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
CAM_I2C_SCL	83	OD	I2C clock of camera		
CAM_I2C_SDA	84	OD	I2C data of camera		

Keypad Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	114	DI	Turn on/off the module	V_{IL}max = 0.60 V V_{IH}min = 1.30 V	Pulled up to VBAT internally. Active low.
RESET_N	225	DI	Reset the module	V_{IL}max = 0.60 V V_{IH}min = 1.30 V	Pulled up to VBAT internally. Active low. Disabled by default and can be enabled by software configuration.
VOL_UP	95	DI	Volume up	V_{IL}max = 0.60 V V_{IH}min = 1.30 V	Pulled up to VBAT internally. Active low.

VOL_DOWN	96	DI	Volume down	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	If it is not used, keep it open. 1.85 V power domain.
RGB LED Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGB_B	249	AI	LED (-)		Connect it to the negative pole of LED. The maximum current is 27.7 mA.
RGB_R	252	AI	LED (-)		Connect it to the negative pole of LED. The maximum current is 27.7 mA.
RGB_G	253	AI	LED (-)		Connect it to the negative pole of LED. The maximum current is 27.7 mA.
SENSOR_I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor		1.85 V power domain. Can be used for other I2C devices.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor		
I2C4 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C4_SDA	106	OD	I2C4 data		1.85 V power domain.
I2C4_SCL	105	OD	I2C4 clock		1.85 V power domain.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	128	AI	General-purpose ADC interface		The maximum input voltage is 1.2 V.
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

BAT_SNS	133	AI	Battery voltage detect		The maximum input voltage is 4.50 V.
CS_M	183	AI	Fuel gauge detect (-)		If fuel gauge is not used, connect these pins to ground.
CS_P	184	AI	Fuel gauge detect (+)		
BAT_THERM	134	AI	Battery temperature detect		Externally pull this pin up to LDO1_1V85 with a 47 kΩ resistor. Supports 10 kΩ NTC thermistor by default - connect this pin to the 10 kΩ NTC thermistor. If unused, connect it to GND with a 10 kΩ resistor.
BAT_ID	185	AI	Battery type detect		Input voltage: 0–1.2 V. If not used, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	87	AIO	Main antenna interface		50 Ω impedance.
ANT_DRX	131	AI	Rx-diversity antenna interface		
ANT_GNSS	121	AI	GNSS antenna interface		
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_87	33	DIO	General-purpose input/output	V_{IL}max = 0.48 V V_{IH}min = 1.39 V V_{OL}max = 0.20 V V_{OH}min = 1.46 V	
GPIO_86	90	DIO	General-purpose input/output		
GPIO_85	97	DIO	General-purpose input/output		
GPIO_88	98	DIO	General-purpose input/output		

GPIO_49	99	DIO	General-purpose input/output	
GPIO_48	100	DIO	General-purpose input/output	
GPIO_156	101	DIO	General-purpose input/output	
GPIO_22	102	DIO	General-purpose input/output	
GPIO_23	103	DIO	General-purpose input/output	
GPIO_28	104	DIO	General-purpose input/output	
GPIO_154	105	DIO	General-purpose input/output	
GPIO_155	106	DIO	General-purpose input/output	
GPIO_52	107	DIO	General-purpose input/output	
GPIO_07	108	DIO	General-purpose input/output	Can be multiplexed into PWMC.
GPIO_54	109	DIO	General-purpose input/output	
GPIO_55	110	DIO	General-purpose input/output	
GPIO_122	112	DIO	General-purpose input/output	Can be multiplexed into EXTINT12.
GPIO_30	113	DIO	General-purpose input/output	
GPIO_29	115	DIO	General-purpose input/output	
GPIO_93	116	DIO	General-purpose input/output	Can be multiplexed into EXTINT8.
GPIO_90	117	DIO	General-purpose input/output	Can be multiplexed into EXTINT5.
GPIO_92	118	DIO	General-purpose input/output	Can be multiplexed into EXTINT7.
GPIO_91	119	DIO	General-purpose input/output	Can be multiplexed into EXTINT6.
GPIO_32	123	DIO	General-purpose input/output	
GPIO_08	124	DIO	General-purpose input/output	

GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_7	260	DO	Generic RF control		
GRFC_5	262	DO	Generic RF control		
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	46	DI	Force the module into emergency download mode	V_{IL}max = 0.48 V V_{IH}min = 1.39 V	You can force the module to enter emergency download mode by pulling it down to ground during power-up.
VIB_DRV_P	28	PO	Motor drive	V_O = 1.80–3.30 V $I_O$max = 100 mA	Connect it to the positive pole of the motor.
Reserved Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	32, 126, 127, 153, 154, 155, 157, 158, 159, 160, 161, 163, 164, 165, 166, 167, 168, 169, 170, 175, 177, 178, 179, 180, 181, 182, 186, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 205, 232, 239, 242, 246, 254, 257, 263, 264, 265, 267, 270				Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides two VBAT_RF pins and two VBAT_BB pins for connection with the external power supply. The VBAT_RF pins are used for the RF part of the module and the VBAT_BB pins are used for the baseband part of the module.

3.4.2. Voltage Stability Requirements

The power supply range of the module is 3.50–4.20 V, and the recommended value is 3.80 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3 A. If the power supply capacity is not sufficient, there will be the risk that the voltage drops below 3.25 V and as a result the module powers off automatically. Therefore, please ensure the input voltage will never drop below 3.25 V.

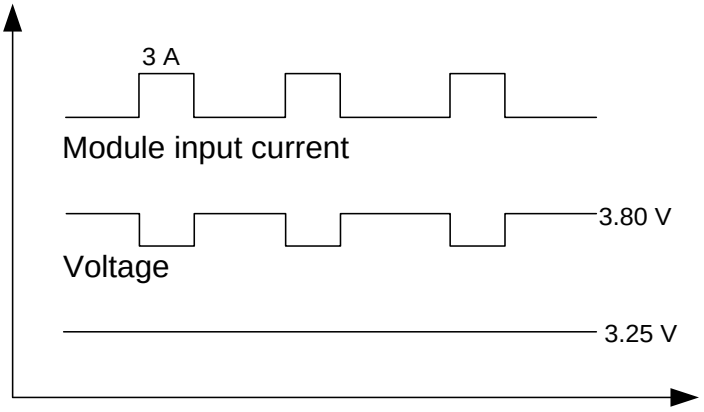


Figure 3: Voltage Drop Sample

To ensure that the supply voltage of the module will not drop below 3.25 V, use a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array and place these capacitors close to VBAT_BB/VBAT_RF pins. Additionally, add a 4.7 μF capacitor in parallel. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

In addition, in order to get a stable power source, it is suggested to use a TVS diode of at least 500 W and place it as close to the VBAT_BB/VBAT_RF pins as possible to enhance surge protection. The following figure shows the star structure of the power supply.

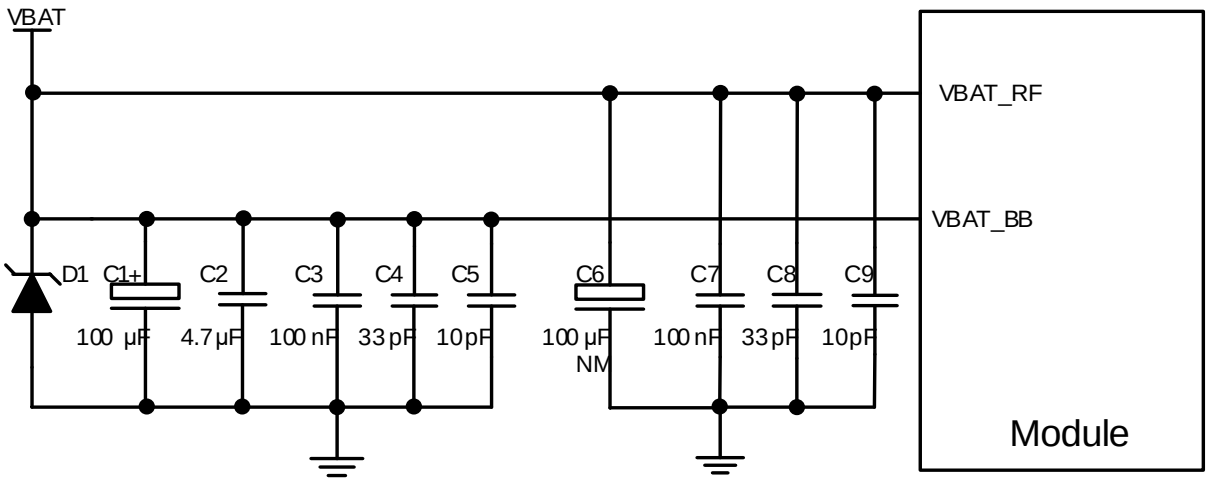


Figure 4: Star Structure of Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3 A. If the voltage difference between the input and output is not too big, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source.

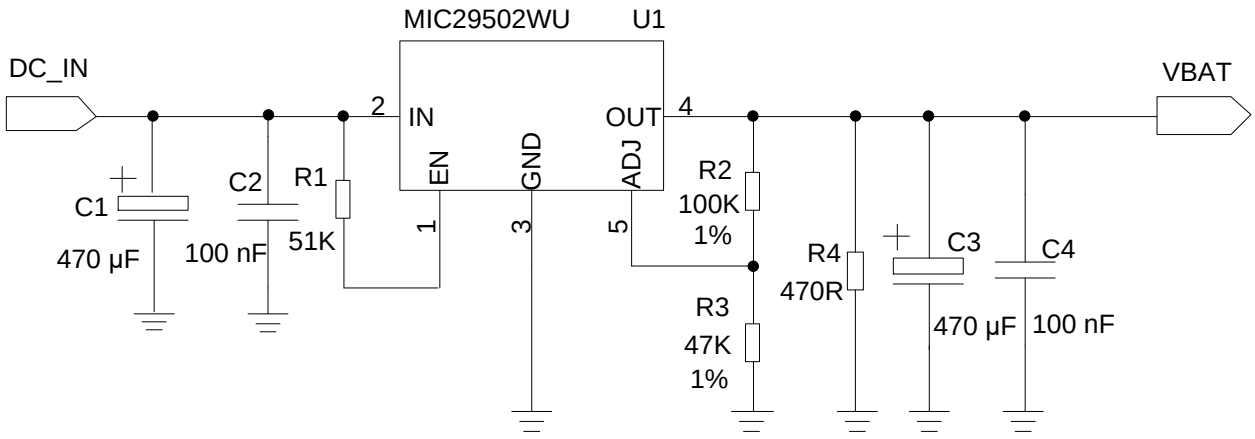


Figure 5: Reference Circuit of Power Supply

NOTE

1. It is recommended to switch off the power supply when the module is in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software, or connect VBAT to a Schottky diode in series to avoid the reverse current to the power supply IC.

3.5. Turn On and Off the Module

3.5.1. Turn On the Module with PWRKEY

You can turn on the module by driving the PWRKEY pin low for at least 2.5 s. PWRKEY pin is pulled up to VBAT internally. It is recommended to use an open drain/collector driver to control the PWRKEY pin. A simple reference circuit is illustrated in the following figure.

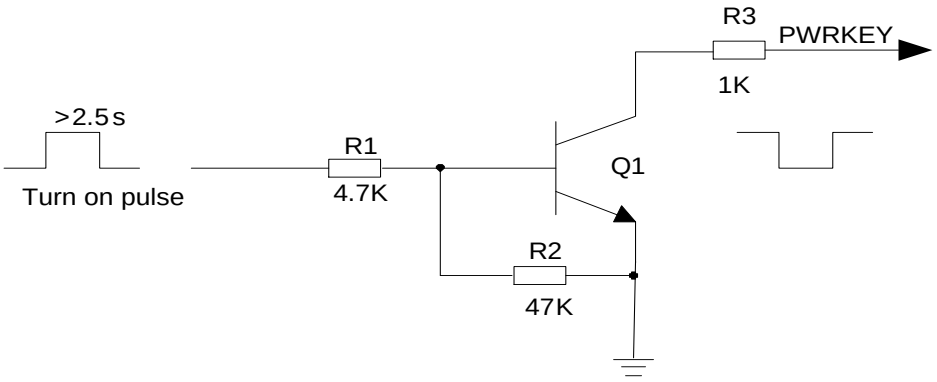


Figure 6: Turn On the Module Using Driving Circuit

The other way to control the PWRKEY pin is by using a button directly. You must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

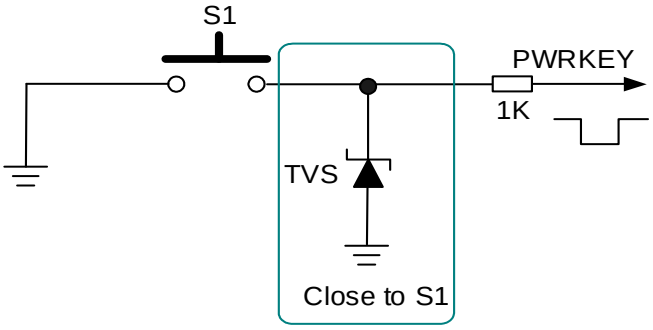


Figure 7: Turn On the Module Using Keystroke

The turning-on scenario is illustrated in the following figure.

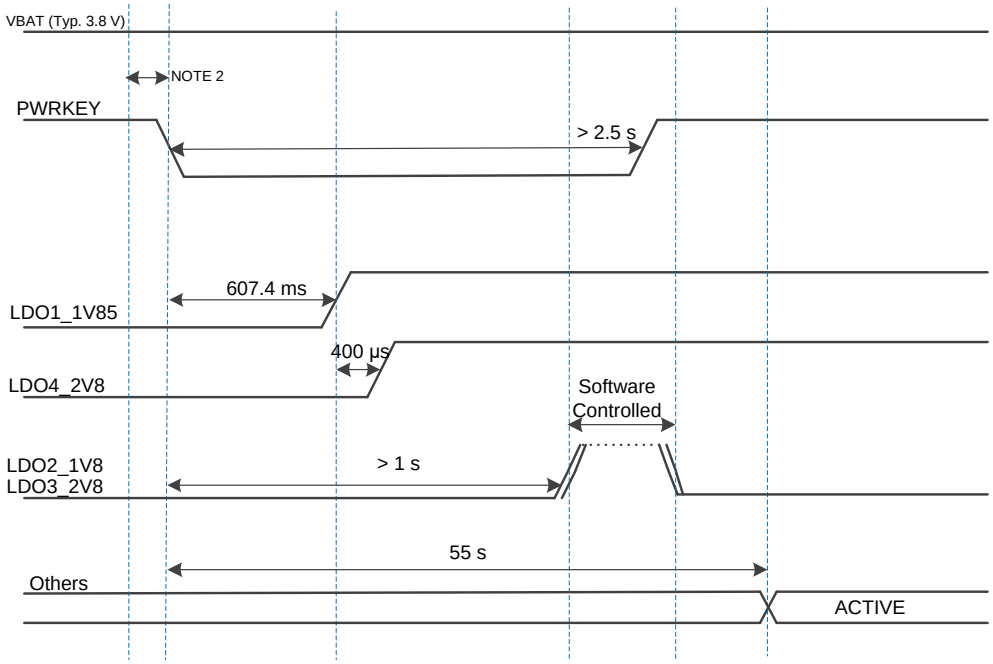


Figure 8: Power-Up Timing

NOTE

1. When the module is powered on for the first time, its timing of power-up may be different from that shown above.
2. Make sure that VBAT is stable before pulling down PWRKEY. It is recommended to wait until VBAT to be stable at 3.8 V for at least 30 ms before pulling down PWRKEY. Additionally, PWRKEY cannot be kept pulled down all the time.

3.5.2. Turn Off/Restart the Module

To turn off the module, you should drive the PWRKEY pin low for at least 1 s and then choose to turn off the module when the prompt window comes up.

It can also be forced to restart by pulling down the PWRKEY key for at least 7 s. The restart timing is as follows:

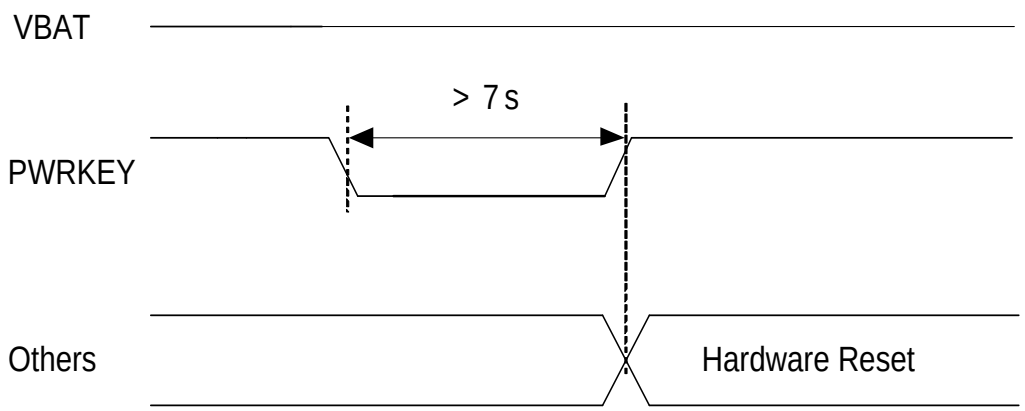


Figure 9: Restart Timing

3.6. Power Output

The module supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 33 pF and a 10 pF capacitor in parallel in the circuit to suppress high-frequency noise.

Table 8: Power Description

Pin Name	Default Voltage (V)	Driving Current (mA)	@ Idle State
LDO1_1V85	1.85	100	Keeps ON
LDO2_1V8	1.80	200	-
LDO3_2V8	2.80	150	-
LDO4_2V8	2.80	200	Keeps ON
SD_VDD	3.00	400	-
USIM1_VDD	1.80/2.95	50	-

USIM2_VDD	1.80/2.95	50	-

3.7. Battery Charging and Management

The module supports battery charging and the charger IC supports trickle charging, constant current charging and constant voltage charging modes.

- **Trickle charging**: There are two steps in this mode. When the battery voltage is between 1.1 V and 2.05 V, a 70 mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.05 V and 3.05 V, the charging current can be set to 450 mA maximally.
- **Constant current mode (CC mode)**: When the battery is increased to between 3.05 V and 4.18 V, the system will switch to CC mode. The charging current is 0.9 A when an adapter is used for battery charging, and the maximum charging current is 450 mA for USB charging.
- **Constant voltage mode (CV mode)**: When the battery voltage reaches the final value 4.18 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, the charging is completed.

Table 9: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_SNS	133	AI	Battery voltage detect	The maximum input voltage is 4.50 V.
CS_M	183	AI	Fuel gauge detect (-)	If fuel gauge is not used, connect these pins to ground.
CS_P	184	AI	Fuel gauge detect (+)	
BAT_THERM	134	AI	Battery temperature detect	Externally pull this pin up to LDO1_1V85 with a 47 kΩ resistor. Supports 10 kΩ NTC thermistor by default - connect this pin to the 10 kΩ NTC thermistor. If unused, connect it to GND with a 10 kΩ resistor.
BAT_ID	185	AI	Battery type detect	Input voltage: 0–1.2 V. If not used, keep it open.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (10 kΩ 1 % NTC thermistor with a B-constant of 3380 K by default and the thermistor should be connected to the BAT_THERM pin. If the BAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for battery charging circuit is shown as below.

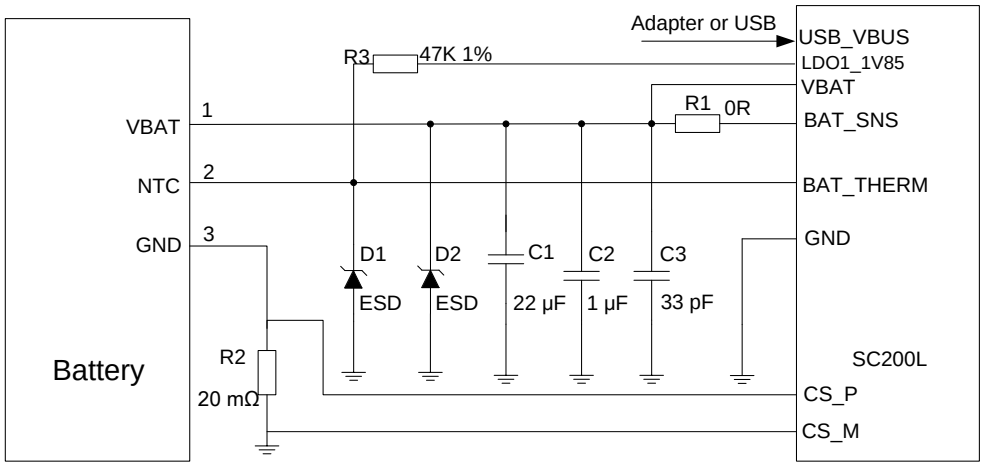


Figure 10: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. For different batteries, you need to modify the charging and discharging curve correspondingly to achieve the best performance.

If the thermistor is not available in the battery, or an adapter is utilized for powering the module, you must connect BAT_THERM to GND via a 10 kΩ resistor. Otherwise, the system may misjudge that the battery temperature is abnormal, and therefore causes battery charging failure.

BAT_SNS must be connected. Otherwise, the module will have trouble in voltage detection, as well as associated module power-on/off issues and battery charging/discharging issues.

The module supports current sensing fuel gauge by default, and conducts current sampling through a 20 mΩ sampling resistor R2.

3.8. USB Interfaces

The module contains two integrated Universal Serial Bus interfaces which comply with the USB 2.0 specification. The USB1 interface supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. It supports USB OTG mode but does not support USB hub. The USB1 interface is used for AT command communication, data transmission, software debugging and firmware upgrade. The USB2 interface supports USB host mode only and supports USB hub. The maximum rate is 100 Mbps.

The following table shows the pin definition of USB1.

Table 10: Pin Definition of USB1 Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	Charging power input; USB 5 V power input; USB/adaptor insertion detect	Vmax = 9.20 V Vmin = 4.50 V Vnom = 5.00 V
USB_DM	13	AIO	USB differential data bus (-)	USB 2.0 standard compliant. 90 Ω differential impedance. Supports USB OTG mode, but does not support USB hub.
USB_DP	14	AIO	USB differential data bus (+)	
USB_ID	16	DI	USB ID detect	High level by default. If not used, keep it open.

For the design of USB 2.0 interface, it is recommended to connect the module's USB_ID directly to the USB_ID pin of the USB connector for USB ID detection. When a device is plugged into the external Micro USB connector, the USB_ID pin of the module will be pulled down to make the module enter host mode.

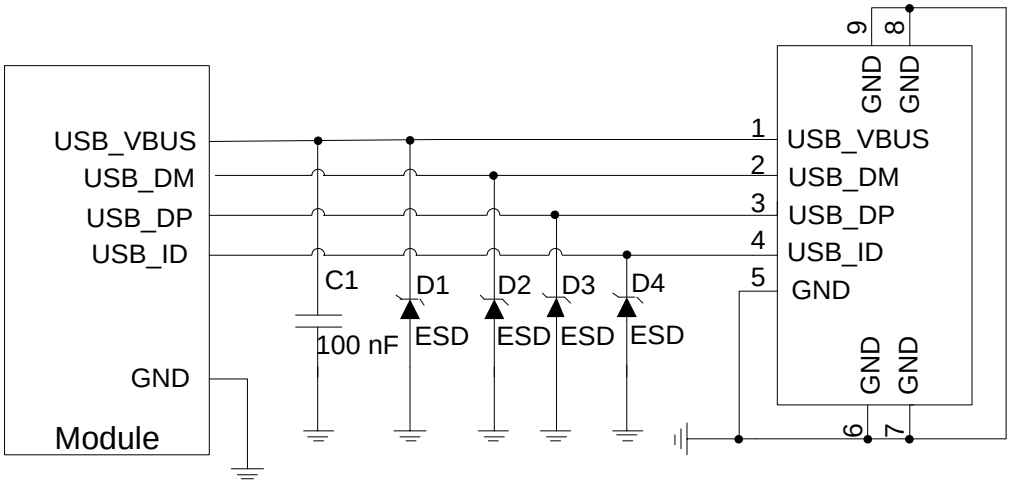


Figure 11: Reference Design for USB1 Interface

The USB1 interface of the module supports OTG function. If you need this function, follow the design below to add an external 5 V power supply, which can provide 500 mA current.

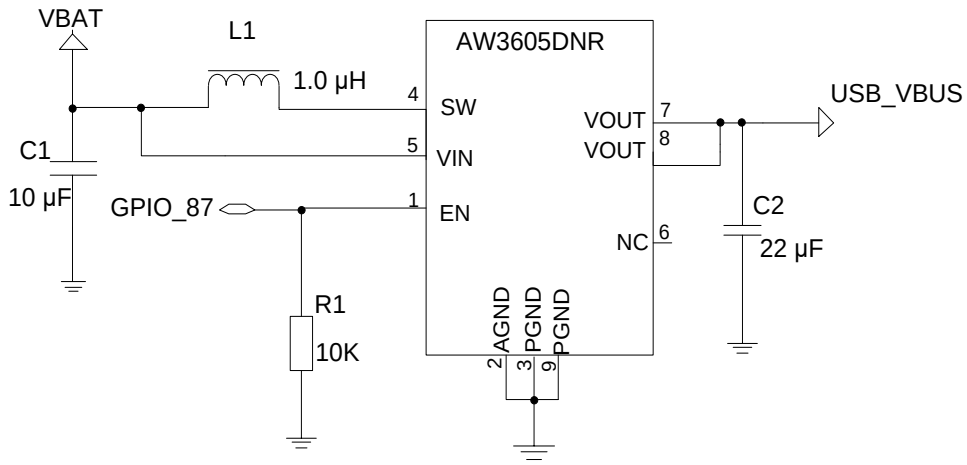


Figure 12: Reference Design for USB1 Power Supply

The following table shows the pin definition of USB2.

Table 11: Pin Definition of USB2 Interface

Pin Name	Pin No.	I/O	Description	Comment
HUB_USB_DP	173	AIO	USB differential data bus (+)	USB 2.0 standard compliant. 90 Ω differential impedance. Supports USB host mode only and supports USB hub.
HUB_USB_DM	174	AIO	USB differential data bus (-)	

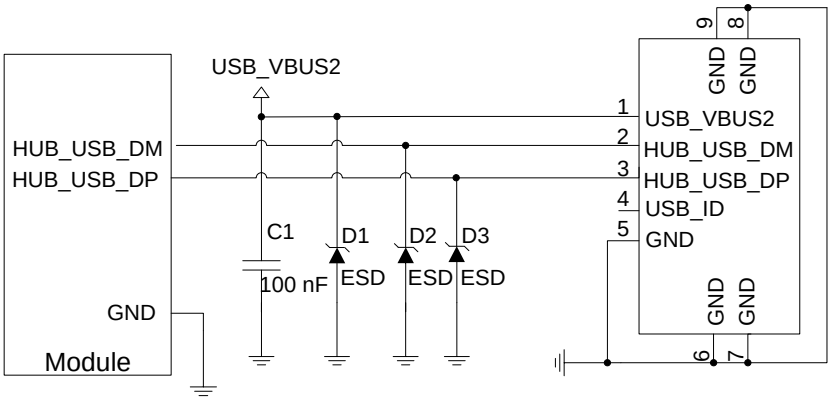


Figure 13: Reference Design for USB2 Interface

The USB2 interface of the module only supports USB host mode. If you need this function, follow the design below to add an external 5 V power supply, which can provide 500 mA current.

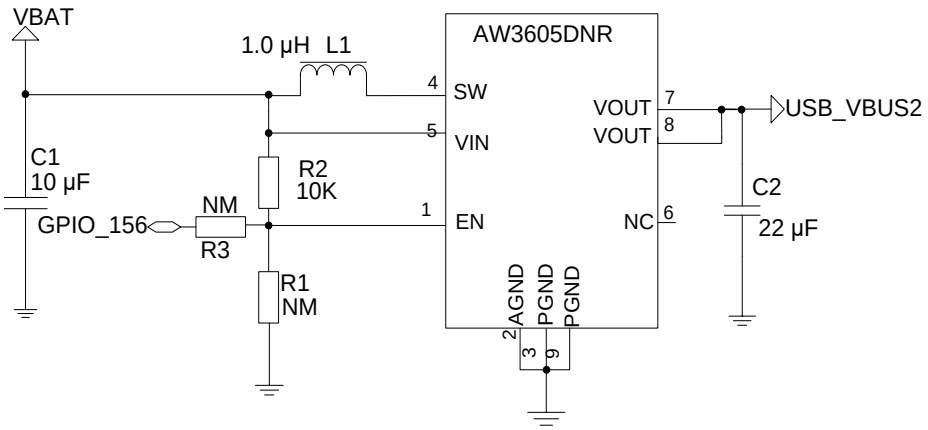


Figure 14: Reference Design for USB2 Power Supply

To ensure USB performance, please comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential traces is 90 Ω.
- Keep the ESD protection devices as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection devices on USB data traces. Typically, the capacitance value should be less than 2 pF.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. Route the USB differential traces in inner-layer with ground shielding on not only the upper and lower layers but also the right and left sides.
- Make sure the trace length difference of USB 2.0 differential data traces is less than 0.7 mm.

Table 12: USB Trace Length Inside the Module

Pin	Signal	Length (mm)	Length Difference (DP - DM)
13	USB_DM	14.94	0.48
14	USB_DP	15.42	
173	HUB_USB_DP	17.66	-0.12
174	HUB_USB_DM	17.78	

3.9. UART Interfaces

The module provides the following two UART interfaces:

- **UART0**: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 3.25 Mbps
- **Debug UART**: 2-wire UART interface, used for debugging by default

The following table shows the pin definition of UART interfaces.

Table 13: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART0_TXD	34	DO	UART0 transmit	1.85 V power domain. If not used, keep these pins open.
UART0_RXD	35	DI	UART0 receive	
UART0_CTS	36	DI	DCE clear to send	
UART0_RTS	37	DO	DCE request to send	
DBG_RXD	93	DI	Debug UART receive	
DBG_TXD	94	DO	Debug UART transmit	

UART0 is a 4-wire UART interface with 1.85 V power domain. A level translator should be used if your application is equipped with a 3.3 V UART interface.

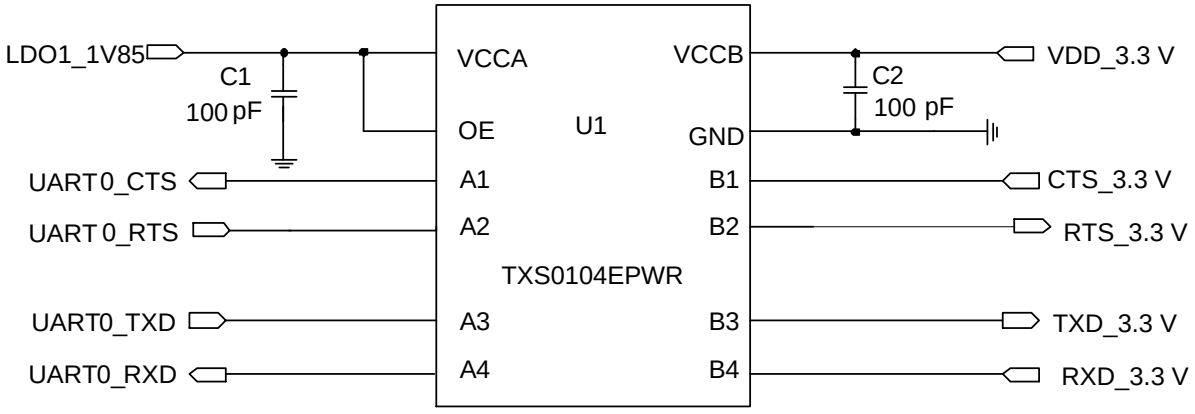


Figure 15: Reference Circuit with Level Translator Chip (for UART0)

The following figure is an example of connection between the module and PC. A voltage level translator and an RS-232 level translator chip are recommended to be added between the module and PC, as shown below:

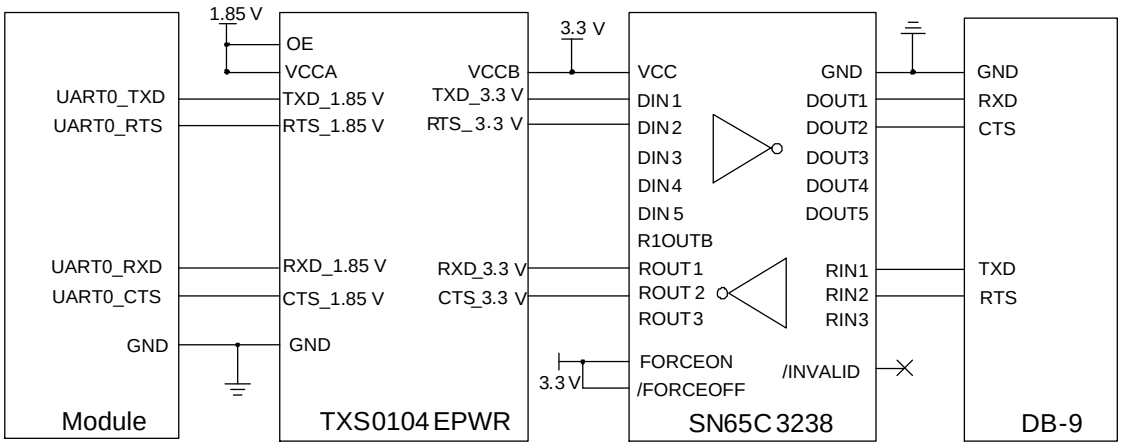


Figure 16: RS-232 Level Match Circuit (for UART0)

3.10. (U)SIM Interfaces

The module provides two (U)SIM interfaces that meet ETSI and IMT-2000 requirements. Dual SIM Card Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card interfaces are powered by the internal power supply of the module.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	This function is enabled by default. Active low. If it is not used, keep it open.
USIM2_RST	18	DO	(U)SIM2 card reset	
USIM2_CLK	19	DO	(U)SIM2 card clock	
USIM2_DATA	20	DIO	(U)SIM2 card data	
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	This function is enabled by default. Active low. If it is not used, keep it open.

USIM1_RST	23	DO	(U)SIM1 card reset	
USIM1_CLK	24	DO	(U)SIM1 card clock	
USIM1_DATA	25	DIO	(U)SIM1 card data	
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.

The module supports (U)SIM card hot-plug function through USIM_DET (The function is enabled by default through software configuration). A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

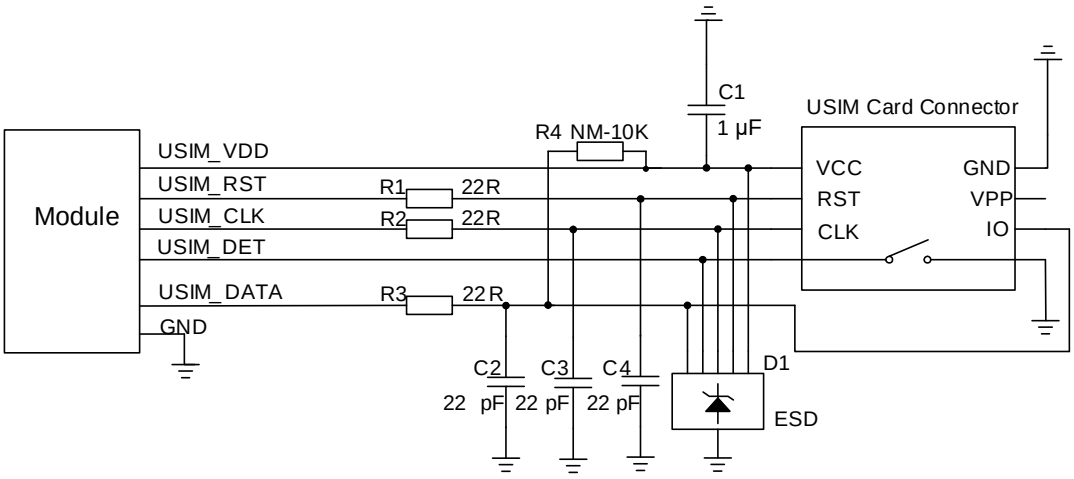


Figure 17: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If USIM_DET is not used, keep it open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

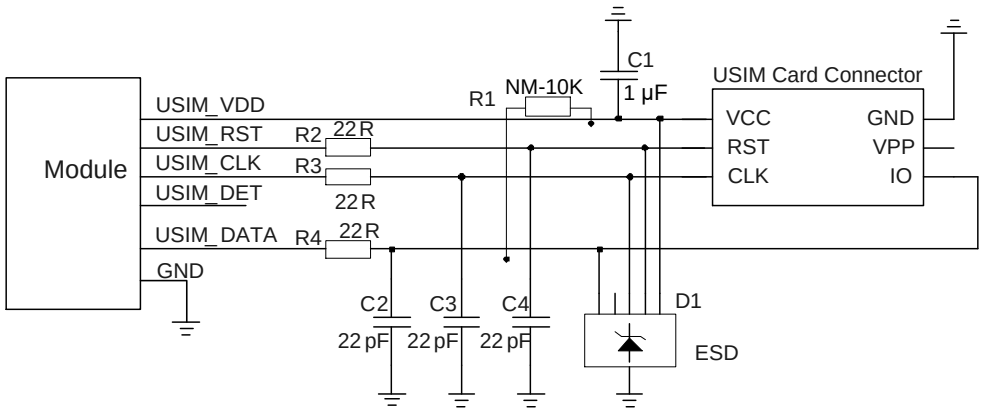


Figure 18: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

To ensure better performance and avoid damage to (U)SIM cards, please follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- In order to ensure good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50 pF. Add 22 Ω resistors in series between the module and (U)SIM card to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- Add 22 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST signal lines to filter RF interference, and place them as close to the (U)SIM card connector as possible.

3.11. SD Card Interface

The module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Pin Description	Comment
SD_CLK	39	DO	SD card clock	50 Ω characteristic impedance.
SD_CMD	40	DIO	SD card command	
SD_DATA0	41	DIO	SDIO data bits	
SD_DATA1	42	DIO		
SD_DATA2	43	DIO		
SD_DATA3	44	DIO		
SD_DET	45	DI	SD card hot-plug detect	Active low.
SD_VDD	38	PO	SD card power supply	If a large-capacity T-Flash card is to be connected, it is recommended to add an LDO which can supply 1 A current.

A reference circuit for SD card interface is shown as below.

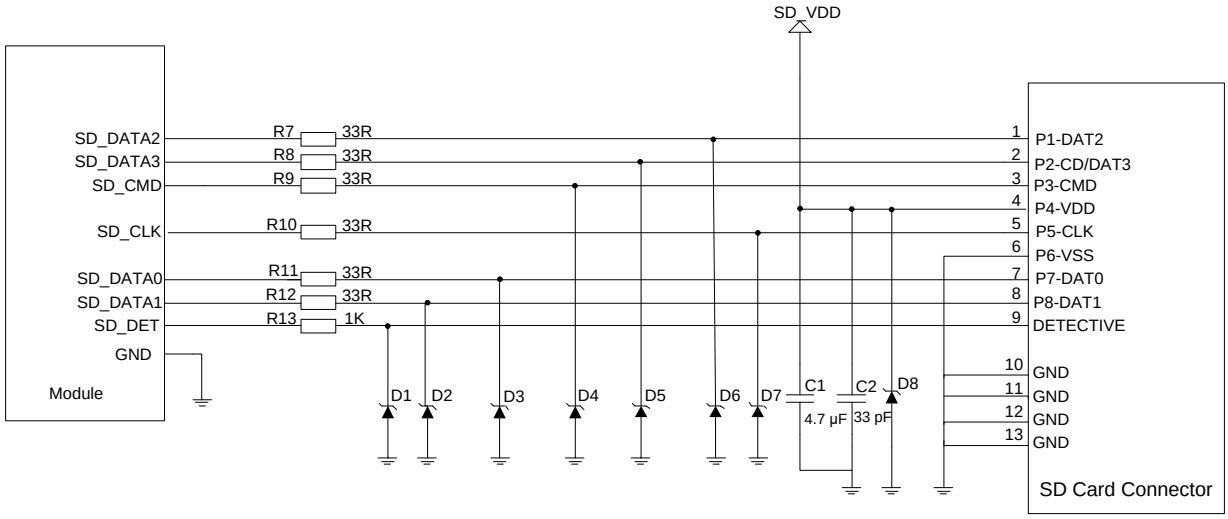


Figure 19: Reference Circuit for SD Card Interface

SD_VDD supplies power for the SD card and can provide up to 400 mA output current. Due to the high output current, it is recommended that the trace width should be 0.5 mm or above. To ensure the stability of output power, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2 and SD_DATA3 are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces to 50 Ω ±10 %, and avoid crossing them with other traces. It is recommended to route the traces on the inner layer of PCB and keep them of the same length. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control the characteristic impedance of these traces to 50 Ω ±10 % and add ground shielding.
- The trace length difference between SD_CLK and other signal traces like SD_CMD and SD_DATA should not exceed 1 mm.

Table 16: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
39	SD_CLK	46.42
40	SD_CMD	46.08
41	SD_DATA0	49.07
42	SD_DATA1	49.62

43	SD_DATA2	47.26	
44	SD_DATA3	49.00	

3.12. GPIO Interfaces

The module has multiple GPIO interfaces with power domain of 1.85 V. The pin definition is listed below.

Table 17: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	Default state [2]	I/O	Pin Description	Comment
GPIO_87	33	IN/PD	DIO	General-purpose input/output	
GPIO_86	90	IN/PU	DIO	General-purpose input/output	
GPIO_85	97	OUT/Hiz	DIO	General-purpose input/output	
GPIO_88	98	IN/PU	DIO	General-purpose input/output	
GPIO_49	99	IN/PU	DIO	General-purpose input/output	
GPIO_48	100	IN/PU	DIO	General-purpose input/output	
GPIO_156	101	IN/PD	DIO	General-purpose input/output	
GPIO_22	102	IN/PD	DIO	General-purpose input/output	
GPIO_23	103	IN/PD	DIO	General-purpose input/output	
GPIO_28	104	IN/PD	DIO	General-purpose input/output	
GPIO_154	105	IN/PD	DIO	General-purpose input/output	
GPIO_155	106	IN/PD	DIO	General-purpose input/output	
GPIO_52	107	IN/PU	DIO	General-purpose input/output	
GPIO_07	108	IN/PD	DIO	General-purpose input/output	Can be multiplexed into PWMC.
GPIO_54	109	IN/PD	DIO	General-purpose input/output	

[2] PD: pull-down; PU: pull-up; IN: input; OUT: output; L: low level; H: high level; Hiz: high impedance..

GPIO_55	110	IN/PD	DIO	General-purpose input/output	
GPIO_122	112	IN/PD	DIO	General-purpose input/output	Can be multiplexed into EXTINT12.
GPIO_30	113	IN/PD	DIO	General-purpose input/output	
GPIO_29	115	IN/PD	DIO	General-purpose input/output	
GPIO_93	116	IN/PD	DIO	General-purpose input/output	Can be multiplexed into EXTINT8.
GPIO_90	117	IN/PU	DIO	General-purpose input/output	Can be multiplexed into EXTINT5.
GPIO_92	118	IN/PD	DIO	General-purpose input/output	Can be multiplexed into EXTINT7.
GPIO_91	119	IN/PD	DIO	General-purpose input/output	Can be multiplexed into EXTINT6.
GPIO_32	123	IN/PD	DIO	General-purpose input/output	
GPIO_08	124	IN/PD	DIO	General-purpose input/output	

NOTE

1. For details of GPIO configuration, see ***document [3]***.
2. For external inputs with hardware mechanical jitter, such as keypad, OTG ID, etc., select GPIOs that can be multiplexed into EXTINT functions.
3. To provide enable signal for ICs like flashlight, switching charger, DC-DC, etc., select GPIOs whose default state is PD.
4. When a non-EXTINT GPIO is used as an interrupt input, wakeup can only be triggered by level (that is, cannot be triggered by edge).

3.13. I2C Interfaces

The module provides four I2C interfaces. All I2C interfaces are open-drain output with pull-up resistors inside the module, and the reference power domain is 1.85 V.

Table 18: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	47	OD	TP I2C clock	Used for touch panel
TP_I2C_SDA	48	OD	TP I2C data	
CAM_I2C_SCL	83	OD	I2C clock of camera	Used for camera
CAM_I2C_SDA	84	OD	I2C data of camera	
I2C4_SCL	105	OD	I2C4 clock	Used for external devices
I2C4_SDA	106	OD	I2C4 data	
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	Used for external sensor
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	

3.14. SPI Interface

The module provides one SPI interface multiplexed from GPIO interfaces. The SPI interface is only supported in master mode and can be used for fingerprint recognition.

Table 19: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
GPIO_93	116	DO	SPI0 clock	Multiplexed into SPI0_CLK
GPIO_90	117	DO	SPI0 chip select	Multiplexed into SPI0_CSN
GPIO_92	118	DI	SPI0 data input	Multiplexed into SPI0_DI
GPIO_91	119	DO	SPI0 data output	Multiplexed into SPI0_DO

3.15. ADC Interface

The module provides one general-purpose analog-to-digital converter (ADC) interface, and the resolution of the ADC is up to 12 bits.

Table 20: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Comment	Pin Name
ADC	128	AI	General-purpose ADC interface	The maximum input voltage is 1.2 V.

3.16. LCM Interface

The module provides an LCM interface, which is MIPI DSI standard compliant. The interface supports high-speed differential data transmission and supports HD+ display (1440 × 720 @ 60 fps). The maximum rate up to 1.5 Gbps/lane. The pin definition of the LCM interface is shown below.

Table 21: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO2_1V8	125	PO	Provides enable signal for external LCD I/O power supply	
LDO4_2V8	156	PO	2.80 V output power supply for LCD VCC	Vnom = 2.80 V $I_O$max = 200 mA
PWM	29	DO	PWM output	Adjusts backlight brightness. 1.85 V power domain.
LCD_RST	49	DO	LCD reset	1.85 V power domain
LCD_TE	50	DI	LCD tearing effect	1.85 V power domain.
DSI_CLK_N	52	AO	MIPI DSI clock (-)	
DSI_CLK_P	53	AO	MIPI DSI clock (+)	
DSI_LN0_N	54	AO	MIPI DSI data 0 (-)	
DSI_LN0_P	55	AO	MIPI DSI data 0 (+)	
DSI_LN1_N	56	AO	MIPI DSI data 1 (-)	

DSI_LN1_P	57	AO	MIPI DSI data 1 (+)
DSI_LN2_N	58	AO	MIPI DSI data 2 (-)
DSI_LN2_P	59	AO	MIPI DSI data 2 (+)
DSI_LN3_N	60	AO	MIPI DSI data 3 (-)
DSI_LN3_P	61	AO	MIPI DSI data 3 (+)

The following are the reference designs for LCM interface.

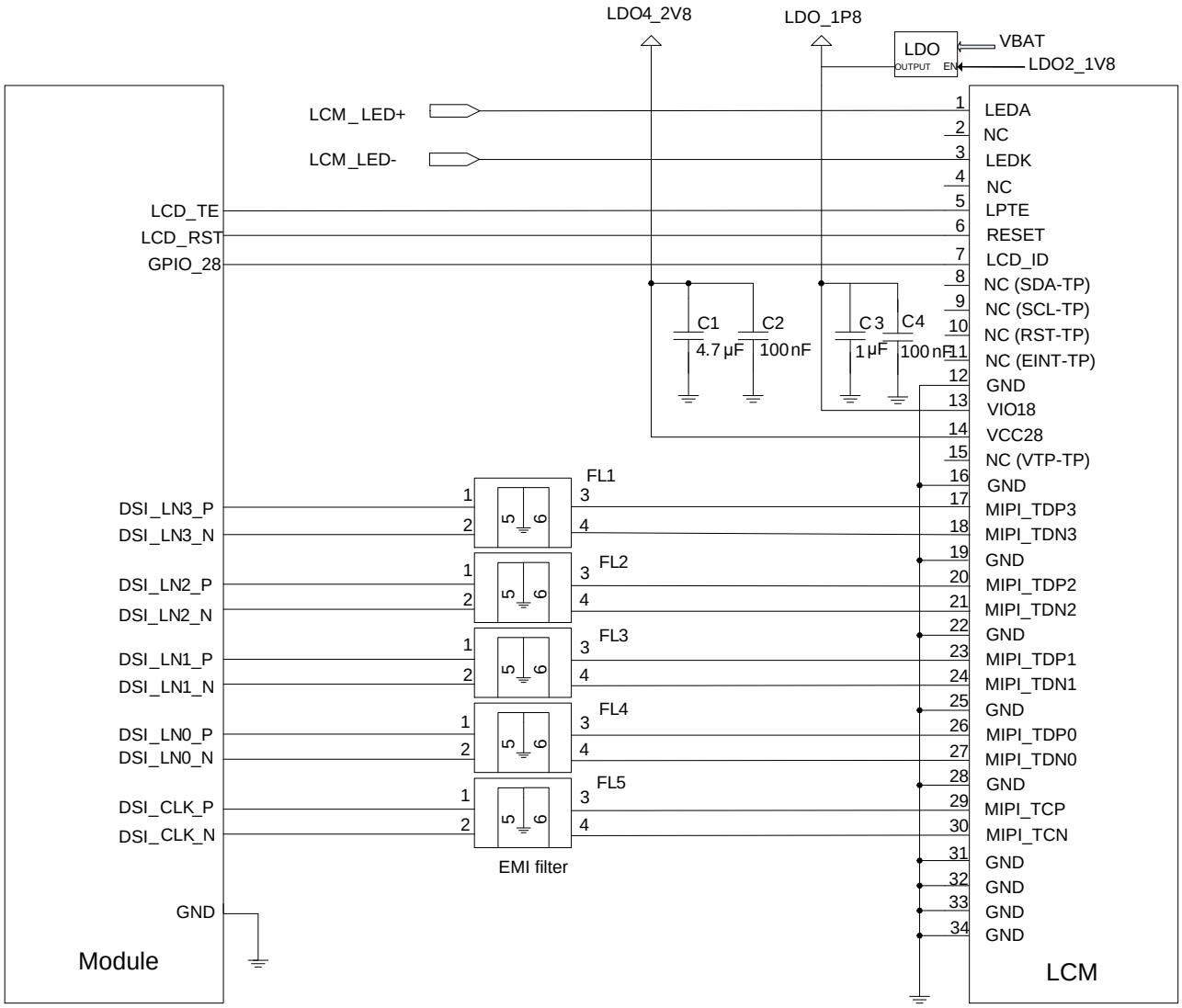


Figure 20: Reference Circuit Design for LCM Interface

MIPI are high-speed signal lines. It is recommended to add common-mode chock in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCM models share the same IC, it is recommended that the LCM module factory burn the OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to GPIO pin of the module and distinguish different factory through level detection.

You can design the external backlight driving circuit for LCM according to actual requirements. A reference circuit design is shown in the following figure, in which the PWM pin is used to adjust the backlight brightness.

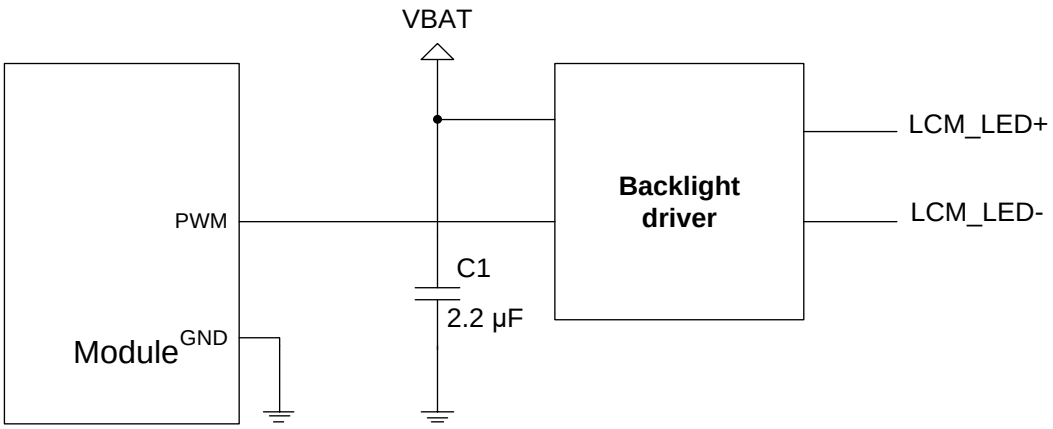


Figure 21: Reference Design of LCM External Backlight Driving Circuit

3.17. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 22: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO4_2V8	156	PO	2.80 V output power supply for TP VDD	Vnom = 2.80 V $I_O$max = 200 mA
LDO2_1V8	125	PO	1.8 V output power supply for TP I/O power	Vnom = 1.80 V $I_O$max = 200 mA
TP_INT	30	DI	TP interrupt	1.85 V power domain.

TP_RST	31	DO	TP reset	1.85 V power domain. Active low.
TP_I2C_SCL	47	OD	TP I2C clock	1.85 V power domain, Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data	

A reference design for touch panel interface is shown below.

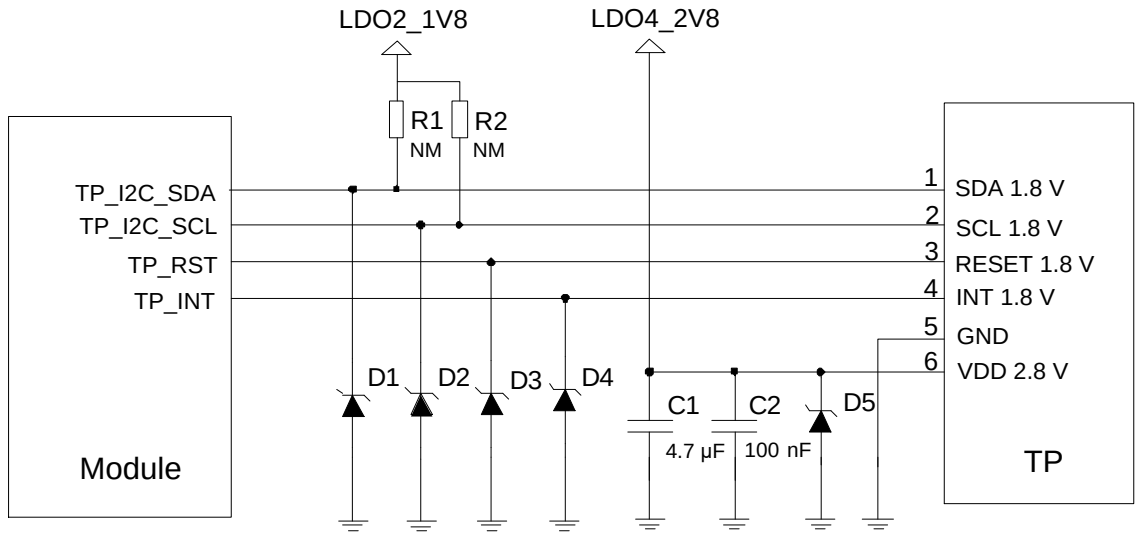


Figure 22: Reference Circuit Design for Touch Panel Interface

NOTE

LDO4_2V8 (keeps ON @ idle state) is used for power supply for TP VDD by default and it can provide 200 mA current.

3.18. Camera Interfaces

Based on MIPI CSI standard, the module supports 2 cameras (2-lane + 1-lane): 1-lane MIPI for front camera which supports up to 2 MP and 2-lane MIPI for rear camera which supports up to 8 MP. The video and photo quality is determined by various factors such as the camera sensor, camera lens quality, etc.

Table 23: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO2_1V8	125	PO	1.80 V output power supply for camera DOVDD	Vnom = 1.80 V $I_O$max = 200 mA
LDO3_2V8	129	PO	2.80 V output power supply for camera AVDD and AFVDD	Vnom = 2.80 V $I_O$max = 150 mA
CSI1_CLK_N	63	AI	MIPI clock of rear camera (-)	
CSI1_CLK_P	64	AI	MIPI clock of rear camera (+)	
CSI1_LN0_N	65	AI	MIPI lane 0 data of rear camera (-)	
CSI1_LN0_P	66	AI	MIPI lane 0 data of rear camera (+)	
CSI1_LN1_N	67	AI	MIPI lane 1 data of rear camera (-)	
CSI1_LN1_P	68	AI	MIPI lane 1 data of rear camera (-)	
CSI0_CLK_N	70	AI	MIPI clock of front camera (-)	
CSI0_CLK_P	71	AI	MIPI clock of front camera (+)	
CSI0_LN0_N	72	AI	MIPI lane 0 data of front camera (-)	
CSI0_LN0_P	73	AI	MIPI lane 0 data of front camera (+)	
MCAM_MCLK	74	DO	Master clock of rear camera	1.85 V power domain.
SCAM_MCLK	75	DO	Master clock of front camera	
MCAM_RST	79	DO	Reset of rear camera	
MCAM_PWDN	80	DO	Power down of rear camera	
SCAM_RST	81	DO	Reset of front camera	
SCAM_PWDN	82	DO	Power down of front camera	
CAM_I2C_SCL	83	OD	I2C clock of camera	
CAM_I2C_SDA	84	OD	I2C data of camera	

The following is a reference circuit design for dual-camera applications.

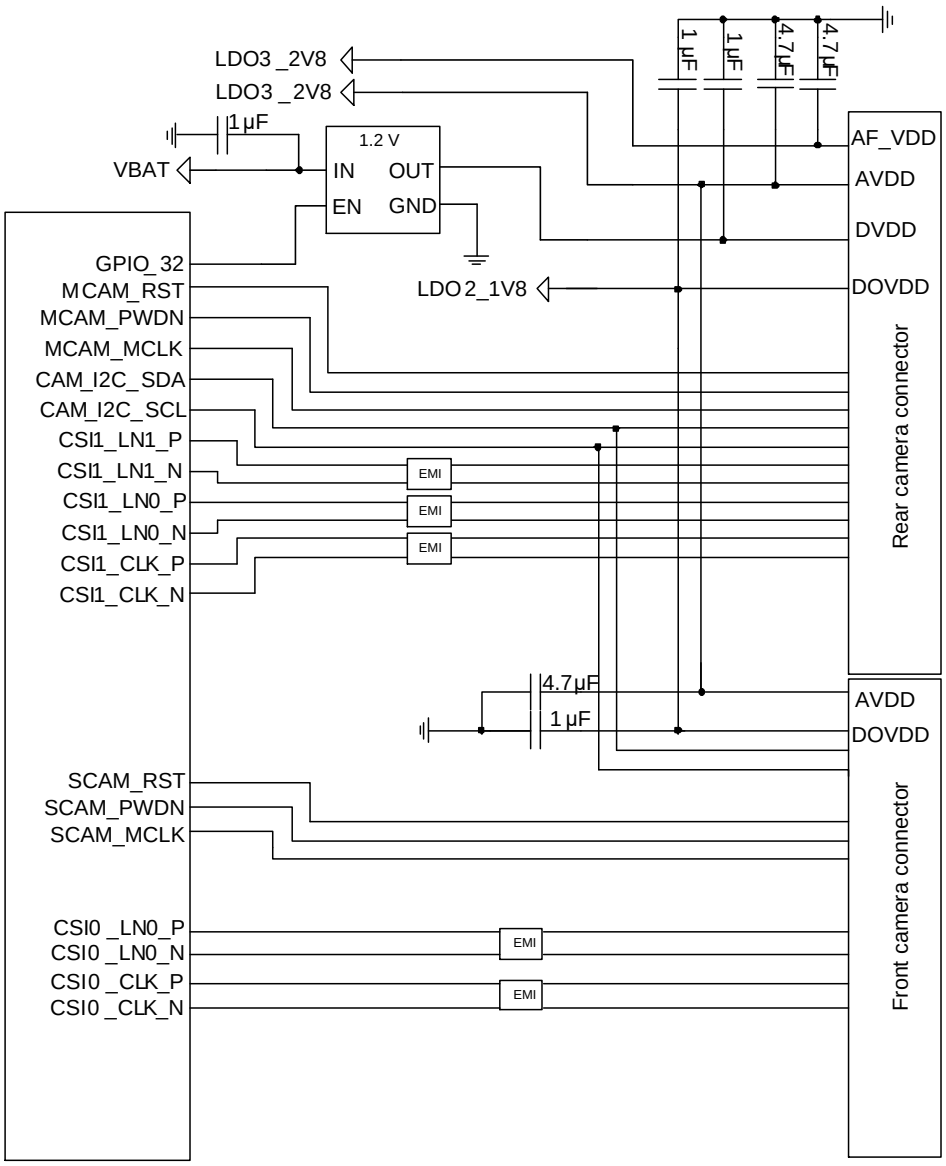


Figure 23: Reference Circuit Design for Dual-Camera Applications

NOTE

CSI1 is used for rear camera, and CSI0 is used for front camera.

3.18.1. MIPI Design considerations

- Pay attention to the pin definitions of LCM and camera connectors to ensure they are connected correctly.
- MIPI are high-speed signal lines, supporting maximum data rate up to 1.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should be of the same length. To avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal lines is recommended. During impedance matching, do not connect GND on different planes to ensure impedance consistency.
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 1 pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 75 mm;
  b) Control the differential impedance within 100 Ω ±10%;
  c) Control intra-lane length difference within 0.5 mm;
  d) Control inter-lane length difference within 1.3 mm.

Table 24: MIPI Trace Length Inside the Module

Pin Name	Pin No.	Length (mm)	Length Difference (P - N)
52	DSI_CLK_N	32.79	-0.22
53	DSI_CLK_P	32.57	
54	DSI_LN0_N	32.90	-0.32
55	DSI_LN0_P	32.58	
56	DSI_LN1_N	32.58	-0.17
57	DSI_LN1_P	32.41	
58	DSI_LN2_N	33.17	0.20
59	DSI_LN2_P	33.37	
60	DSI_LN3_N	35.93	0.30
61	DSI_LN3_P	36.23	
63	CSI1_CLK_N	13.71	-0.15
64	CSI1_CLK_P	13.56	

65	CSI1_LN0_N	14.13	-0.38
66	CSI1_LN0_P	13.75	
67	CSI1_LN1_N	17.45	-0.37
68	CSI1_LN1_P	17.08	
70	CSI0_CLK_N	18.52	0.41
71	CSI0_CLK_P	18.93	
72	CSI0_LN0_N	19.76	0.05
73	CSI0_LN0_P	19.81	

3.19. Sensor Interfaces

The module supports communication with sensors via I2C interfaces, and it supports various sensors such as ALS/PS, accelerometer sensor, gyroscope sensor, geomagnetic sensor, etc.

Table 25: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	1.85 V power domain. Can be used for other I2C devices.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	
GPIO_52	107	DI	ALS/PS sensor interrupt	
GPIO_54	109	DI	Geomagnetic sensor interrupt	
GPIO_55	110	DI	Accelerometer sensor interrupt	
GPIO_07	108	DI	Gyroscope sensor interrupt	

3.20. Audio Interfaces

The module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 26: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	4	AI	Microphone input for channel 1 (+)	
MIC1_N	5	AI	Microphone input for channel 1 (-)	
MIC2_P	6	AI	Microphone input for headset (+)	
MIC2_N	148	AI	Microphone input for headset (-)	
MIC_BIAS2	149	PO	Microphone bias voltage 2	Vmin = 2.20 V Vmax = 3.00 V Vnom = 2.80 V
MIC3_P	152	AI	Microphone input for channel 2 (+)	
MIC3_N	151	AI	Microphone input for channel 2 (-)	
MIC_BIAS1	147	PO	Microphone bias voltage 1	Vmin = 2.20 V Vmax = 3.00 V Vnom = 2.50 V
EAR_P	8	AO	Earpiece output (+)	
EAR_N	9	AO	Earpiece output (-)	
SPK_P	10	AO	Speaker output (+)	
SPK_N	11	AO	Speaker output (-)	
HPH_R	136	AO	Headphone right channel output	
HPH_REF	137	AO	Headphone reference ground	If it is not used, connect it to ground.
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset insertion detect	High level by default.
HPMIC_DET	150	AI	Headphone microphone detect	

- The module has three differential audio input channels.
- The output voltage range of the two MIC_BIAS is programmable between 2.2 V and 3.0 V, and the maximum output current is 2 mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose maximum output power is 0.8 W when the load is 8 Ω.
- The headset interface features stereo left and right channel output, and headset insertion detection function is supported.

3.20.1. Reference Circuit Design for Microphone Interfaces

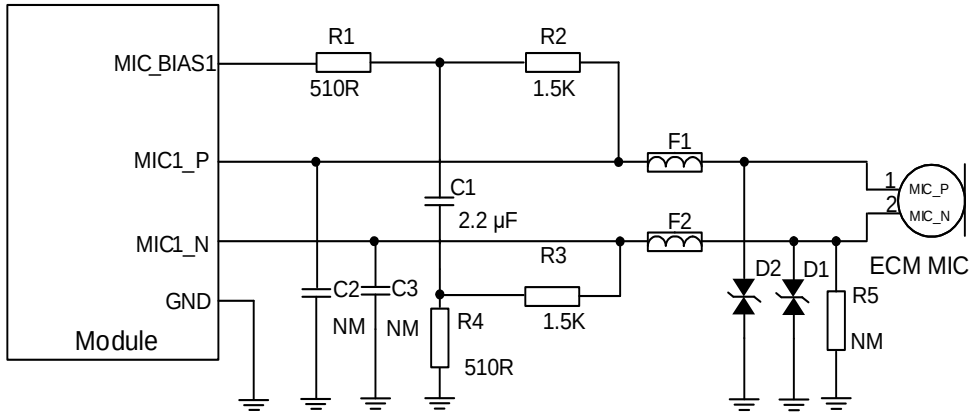


Figure 24: Reference Design for ECM Microphone

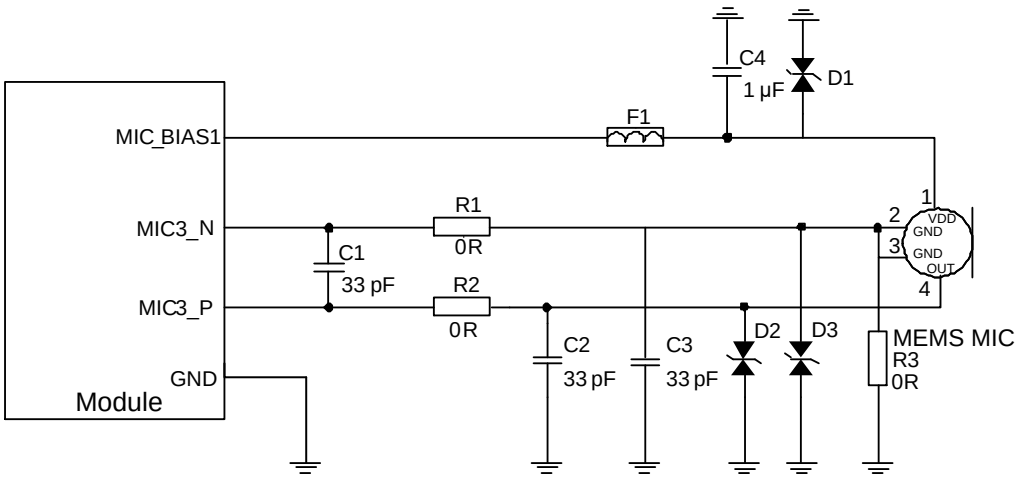


Figure 25: Reference Design for MEMS Microphone

3.20.2. Reference Circuit Design for Earpiece Interface

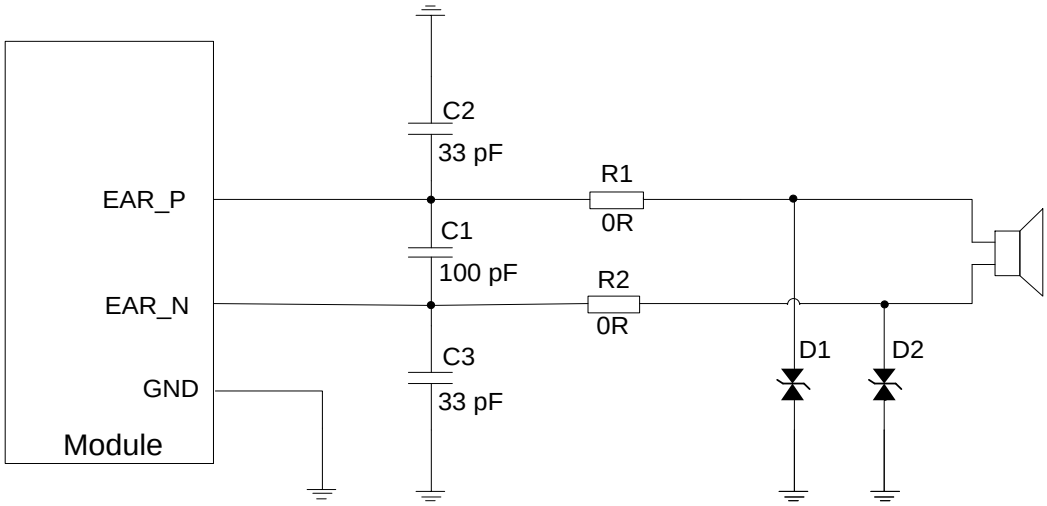


Figure 26: Reference Circuit Design for Earpiece Interface

3.20.3. Reference Circuit Design for Headset Interface

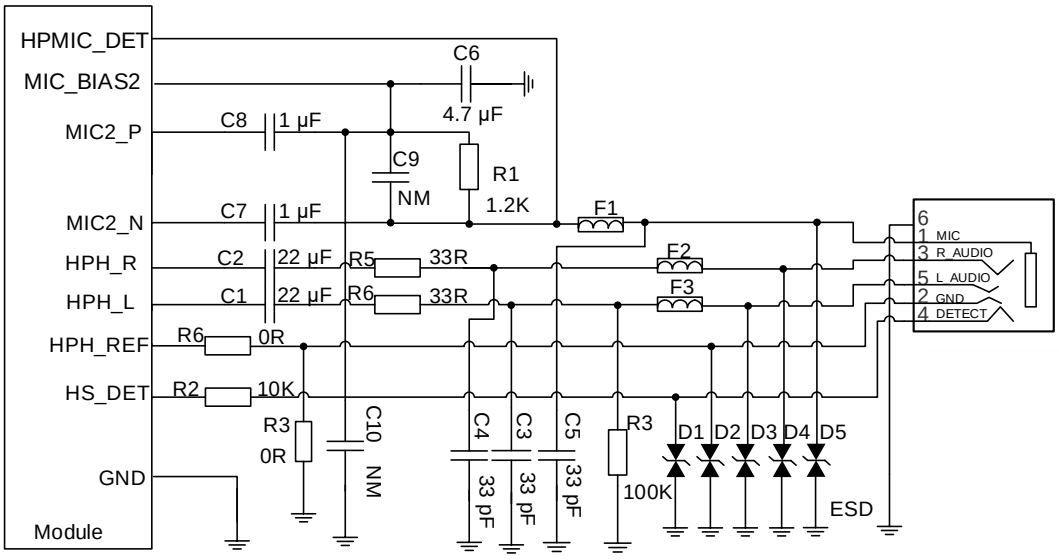


Figure 27: Reference Circuit Design for Headset Interface

3.20.4. Reference Circuit Design for Loudspeaker Interface

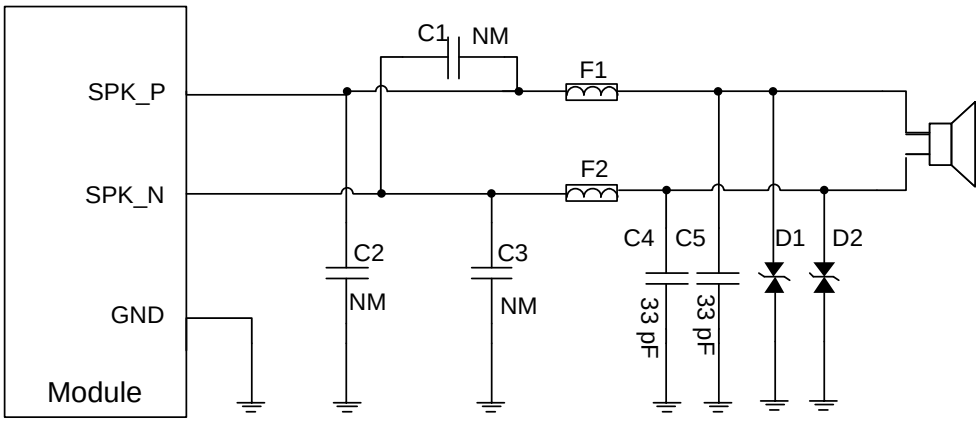


Figure 28: Reference Circuit Design for Loudspeaker Interface

3.20.5. Audio Signal Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out RF interference when the module is transmitting at EGSM900. Without this capacitor, TDD noise could be heard during voice calls. The 10 pF capacitor is used to filter out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you should consult the capacitor vendors to choose the most suitable capacitor to filter out the high-frequency noises.

The severity of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor should be selected based on test results. Sometimes, even no RF filtering capacitor is required. .

To decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Additionally, keep power traces far away from the audio traces and do not route them in parallel.

The differential audio traces must be routed according to differential signal layout rules.

3.21. Emergency Download Interface

USB_BOOT is an emergency download interface. You can force the module to enter emergency download mode by pulling it down to ground during power-up. This is an emergency option when start-up failures or operational abnormalities occur. For firmware upgrade and debugging in the future, please reserve the following reference design.

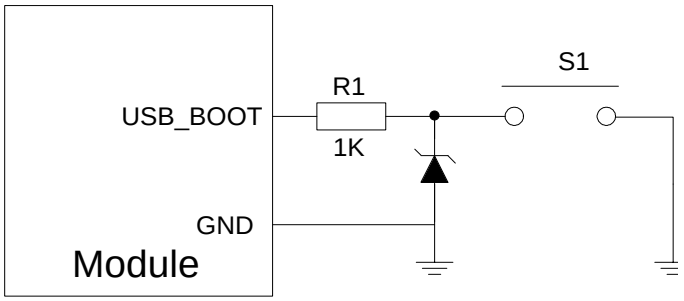


Figure 29: Reference Circuit Design for Emergency Download Interface

NOTE

The reference design above must be applied for firmware upgrade via USB interface.

4 Wi-Fi and Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The impedance of the interface should be controlled to 50 Ω. You may connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via the interface to achieve Wi-Fi and Bluetooth functions.

4.1. Wi-Fi Overview

The module supports 2.4 GHz and 5 GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is 150 Mbps for 2.4 GHz frequency band, and 433 Mbps for 5 GHz frequency band. The features are as below:

- Supports Wake-on-WLAN (WoWLAN)
- Supports ad hoc mode
- Supports WAPI SMS4 hardware encryption
- Supports STA mode
- Supports AP mode
- Supports Wi-Fi Direct
- Supports MCS 0–7 for HT20 and HT40
- Supports MCS 0–8 for VHT20
- Supports MCS 0–9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 27: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	TBD
	802.11b	11 Mbps	TBD
	802.11g	6 Mbps	TBD

	802.11g	54 Mbps	TBD
	802.11n HT20	MCS0	TBD
	802.11n HT20	MCS7	TBD
	802.11n HT40	MCS0	TBD
	802.11n HT40	MCS7	TBD
5 GHz	802.11a	6 Mbps	TBD
	802.11a	54 Mbps	TBD
	802.11n HT20	MCS0	TBD
	802.11n HT20	MCS7	TBD
	802.11n HT40	MCS0	TBD
	802.11n HT40	MCS7	TBD
	802.11ac VHT20	MCS0	TBD
	802.11ac VHT20	MCS8	TBD
	802.11ac VHT40	MCS0	TBD
	802.11ac VHT40	MCS9	TBD
	802.11ac VHT80	MCS0	TBD
	802.11ac VHT80	MCS9	TBD

Table 28: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	TBD
	802.11b	11 Mbps	TBD
	802.11g	6 Mbps	TBD
	802.11g	54 Mbps	TBD
	802.11n HT20	MCS0	TBD

	802.11n HT20	MCS7	TBD
	802.11n HT40	MCS0	TBD
	802.11n HT40	MCS7	TBD
5 GHz	802.11a	6 Mbps	TBD
	802.11a	54 Mbps	TBD
	802.11n HT20	MCS0	TBD
	802.11n HT20	MCS7	TBD
	802.11n HT40	MCS0	TBD
	802.11n HT40	MCS7	TBD
	802.11ac VHT20	MCS0	TBD
	802.11ac VHT20	MCS8	TBD
	802.11ac VHT40	MCS0	TBD
	802.11ac VHT40	MCS9	TBD
	802.11ac VHT80	MCS0	TBD
	802.11ac VHT80	MCS9	TBD

4.2. Bluetooth Overview

The module supports Bluetooth 5.0 (BR/EDR + BLE), as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally supports up to 7 wireless connections.
- Maximally supports up to 3.5 piconets at the same time.
- Supports one SCO or eSCO (Extended Synchronous Connection Oriented) connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 29: Bluetooth Data Rate and Versions

Version	Data rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0+EDR	3 Mbit/s	> 80 kbit/s
4.2	24 Mbit/s	Reference 4.0 LE
5.0	48 Mbit/s	Reference 5.0 LE

Referenced specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016

4.2.1. Bluetooth Performance

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 30: Bluetooth Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	TBD	TBD	TBD
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	TBD	TBD	TBD

5 GNSS

The module integrates a GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, and BeiDou. With an embedded LNA, the positioning accuracy of the module has been significantly improved.

5.1. GNSS Performance

The following table lists the GNSS performance of the module in conduction mode.

Table 31: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Cold start	TBD	dBm
	Reacquisition	TBD	dBm
	Tracking	TBD	dBm
TTFF	Cold start	TBD	s
	Warm start	TBD	s
	Hot start	TBD	s
Static Drift	CEP-50	TBD	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. To avoid these, follow the design rules listed below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, place GNSS RF signal traces and RF components far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. The junction capacitance of the diodes should be less than 0.5 pF. Otherwise, it will influence the impedance characteristic of RF circuit loop or cause attenuation of bypass RF signals.
- Control the impedance of feeder line or PCB trace to 50 Ω, and keep the trace length as short as possible.
- See ***Chapter 6.3*** for reference circuit designs of GNSS antenna.

6 Antenna Interfaces

The module provides four antenna interfaces: main antenna, Rx-diversity antenna, Wi-Fi/Bluetooth antenna, and GNSS antenna respectively. The impedance of the antenna ports should be controlled to 50 Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 32: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	AIO	Main antenna interface	50 Ω impedance.
ANT_DRX	131	AI	Rx-diversity antenna interface	

6.1.1. Module Operating Frequencies

Table 33: SC200L-CE* Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B8	925–960	880–915	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz

LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

Table 34: SC200L-EU Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B5	869–894	824–849	MHz
WCDMA B8	925–960	880–915	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-FDD B20	791–821	832–862	MHz
LTE-FDD B28(A + B)	758–803	703–748	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 35: SC200L-AU* Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869–894	824–849	MHz
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
PCS1900	1930–1990	1850–1910	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B2	1930–1990	1850–1910	MHz
WCDMA B4	2110–2155	1710–1755	MHz
WCDMA B5	869–894	824–849	MHz
WCDMA B8	925–960	880–915	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B2	1930–1990	1850–1910	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz
LTE-FDD B4	2110–2155	1710–1755	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-FDD B28(A + B)	758–803	703–748	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz

6.1.2. Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

A reference circuit design for main and Rx-diversity antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default and the resistors are 0 Ω.

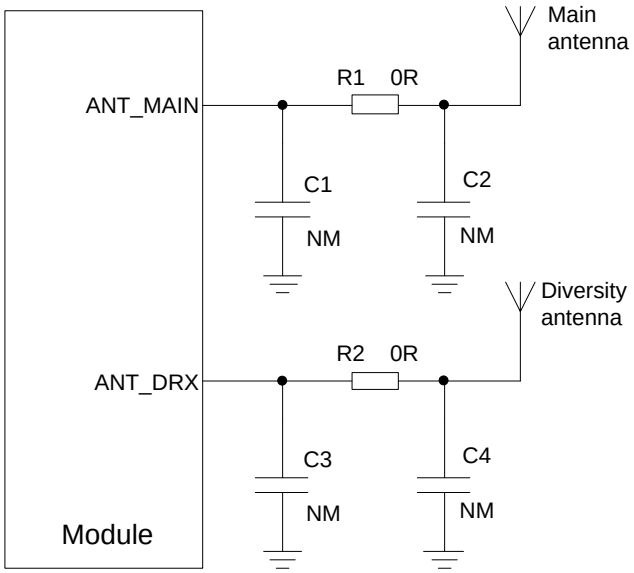


Figure 30: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.2. Wi-Fi/Bluetooth Antenna Interface

Table 36: Pin Definition of Wi-Fi/Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance.

Table 37: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi (2.4 GHz)	2402–2482	MHz
Wi-Fi (5 GHz)	5180–5825	MHz
Bluetooth	2402–2480	MHz

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. A π-type matching circuit is recommended to be reserved for better RF performance. The capacitors are not mounted by default and the resistor is 0 Ω.

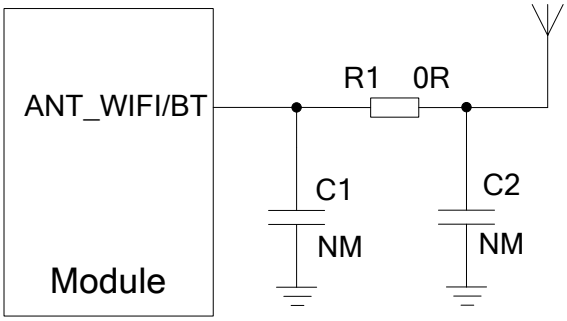


Figure 31: Reference Circuit Design for Wi-Fi/Bluetooth Antenna Interface

6.3. GNSS Antenna Interface

Table 38: Pin Definition of GNSS Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50 Ω impedance.

Table 39: GNSS Frequencies

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
BeiDou	1561.098 ±2.046	MHz

6.3.1. Reference Circuit Design for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

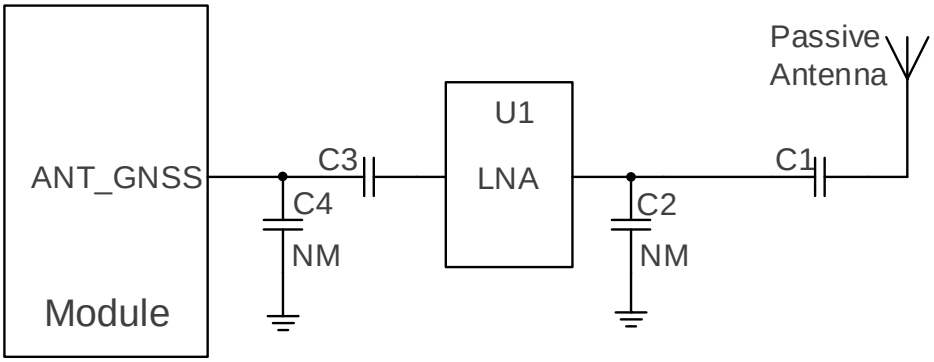


Figure 32: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long) and the external loss is more than 2 dB, it is recommended to add an external LNA circuit for better GNSS receiving performance, and place the LNA close to the antenna.

6.3.2. Reference Circuit Design for Active Antenna

The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high-performance LDO as the power supply. A reference design of GNSS active antenna is shown below.

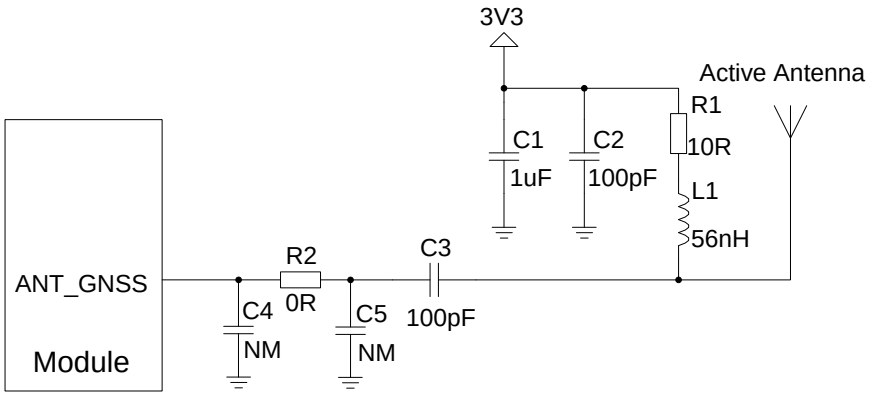


Figure 33: Reference Circuit Design for GNSS Active Antenna

6.5. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

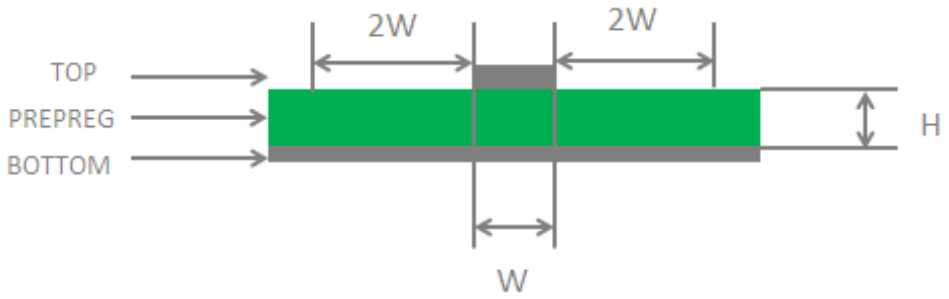


Figure 34: Microstrip Line Design on a 2-layer PCB

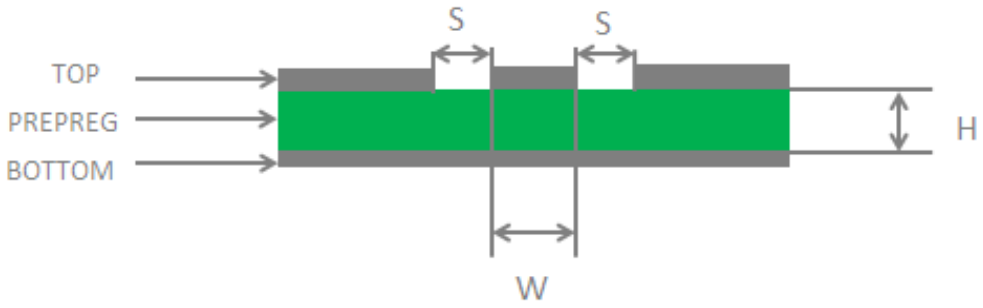


Figure 35: Coplanar Waveguide Line Design on a 2-layer PCB

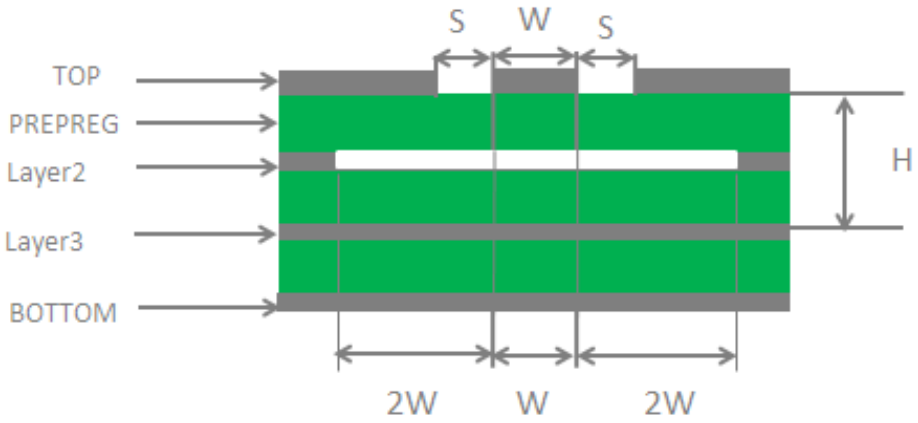


Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

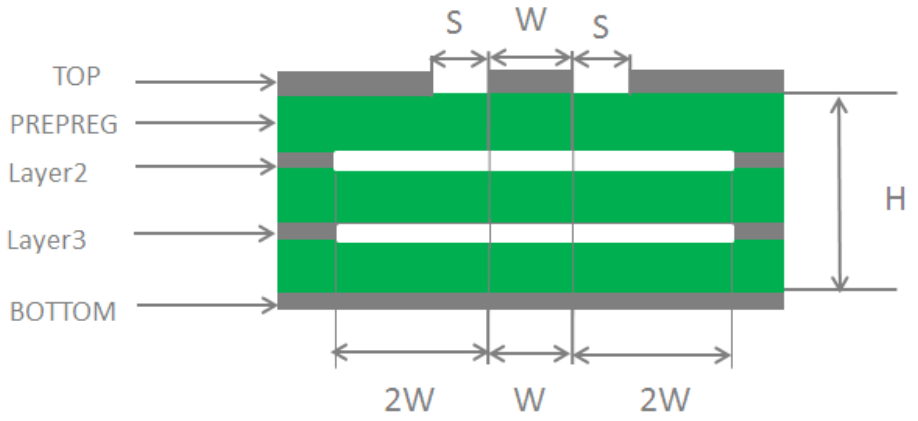


Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- Design the GND pins adjacent to RF pins as thermal relief pads, and fully connect them to ground.
- Keep the distance between the RF pins and the RF connector as short as possible. Change all the right-angle traces to curved ones and the recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- Keep the reference ground of RF traces complete. Meanwhile, add some ground vias around RF traces and the reference ground to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

6.6. Antenna Installation

6.6.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity, Wi-Fi/Bluetooth antenna and GNSS antenna.

Table 40: Antenna Requirements

Type	Requirements
GSM/WCDMA/LTE	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Insertion Loss: < 1 dB (GSM850, EGSM900, WCDMA B5/B8, LTE B5/B8/B20/B28A/B28B) Insertion Loss: < 1.5 dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4/B34/B39) Insertion Loss: < 2 dB (LTE-FDD B7, LTE-TDD B38/B40/B41)
Wi-Fi/Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Insertion Loss: < 1 dB
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi Active Antenna Noise Figure: < 1.5 dB Active Antenna Gain: >-2 dBi Active Antenna Embedded LNA Gain: <17 dB (Typ.) Active Antenna Total Gain: < 17 dBi (Typ.)

6.6.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

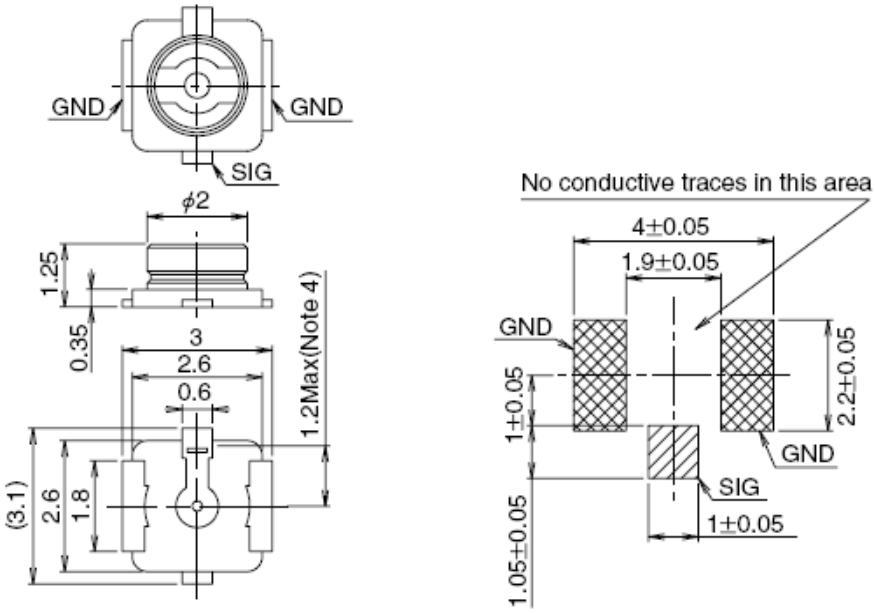


Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

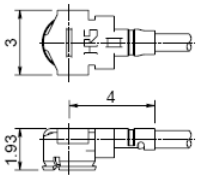
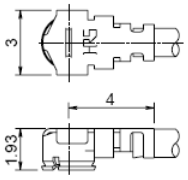
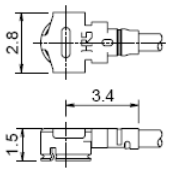
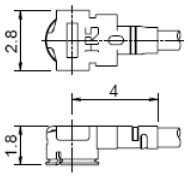
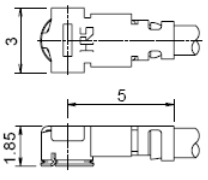
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

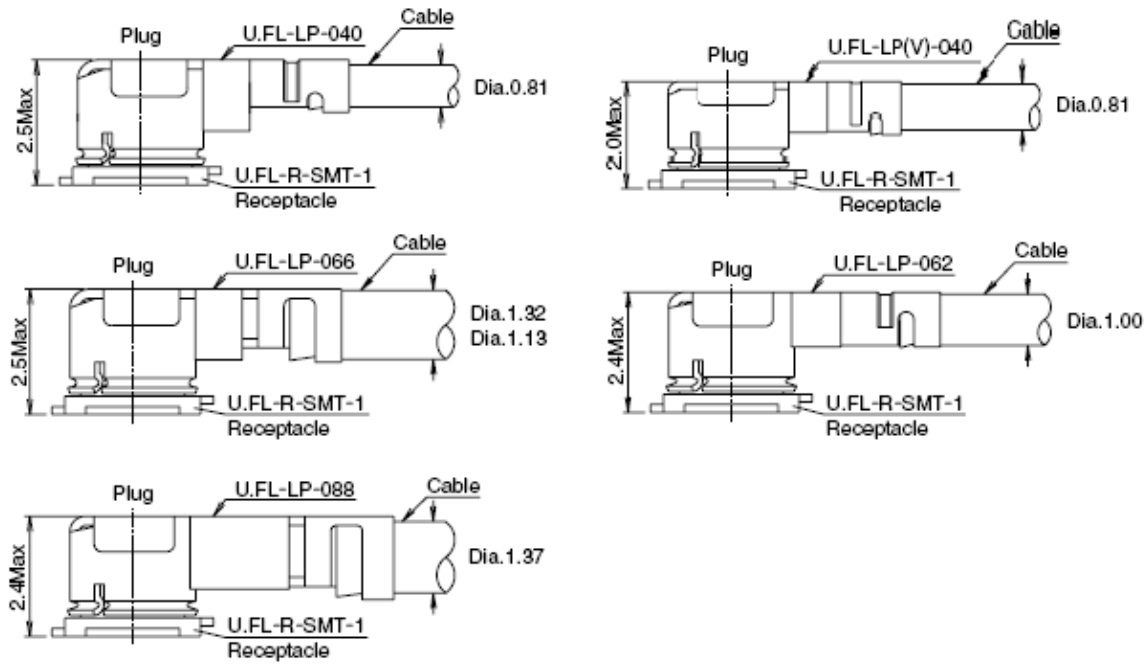


Figure 40: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Reliability, Radio and Electrical Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 41: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	6	V
USB_VBUS	-0.3	16.0	V
Current on VBAT	0	3.0	A
Voltage on Digital Pins	-0.3	1.98	V

7.2. Power Supply Ratings

Table 42: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values	3.50	3.80	4.20	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900	-	-	800	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900	-	1.80	3.0	A
USB_VBUS	-	-	4.50	5.0	9.20	V

7.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 43: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [3]	-30	+25	+75	ºC
Storage Temperature Range	-40	-	+90	ºC

7.4. Power Consumption

Table 44: SC200L-CE* Power Consumption

Description	Conditions	Min	Typ.
OFF state	Power down	TBD	μA
GSM/GPRS supply current	Sleep (USB disconnected) @ DRX = 2	TBD	mA
	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA

[3] Within the operating temperature range, the module is 3GPP compliant.

	Sleep (USB disconnected) @ DRX = 9	TBD	mA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
GSM voice call	EGSM900 @ PCL 5	TBD	mA
	EGSM900 @ PCL 12	TBD	mA
	EGSM900 @ PCL 19	TBD	mA
	DCS1800 @ PCL 0	TBD	mA
	DCS1800 @ PCL 7	TBD	mA
	DCS1800 @ PCL 15	TBD	mA
WCDMA voice call	B1 @ max power	TBD	mA
	B8 @ max power	TBD	mA
GPRS data transfer	EGSM900 (1UL/4DL) @ PCL 5	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 5	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 5	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 5	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 0	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 0	TBD	mA
	DCS1800 (3UL/2DL) @ PCL 0	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 0	TBD	mA

EDGE data transfer	EGSM900 (1UL/4DL) @ PCL 8	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 8	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 8	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 8	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 2	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 2	TBD	mA
	DCS1800 (3UL/2DL) @ PCL 2	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 2	TBD	mA
WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA
	B8 (HSDPA) @ max power	TBD	mA
	B1 (HSUPA) @ max power	TBD	mA
	B8 (HSUPA) @ max power	TBD	mA
LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
	LTE-FDD B3 @ max power	TBD	mA
	LTE-FDD B5 @ max power	TBD	mA
	LTE-FDD B8 @ max power	TBD	mA
	LTE-TDD B34 @ max power	TBD	mA
	LTE-TDD B38 @ max power	TBD	mA
	LTE-TDD B39 @ max power	TBD	mA
	LTE-TDD B40 @ max power	TBD	mA
	LTE-TDD B41 @ max power	TBD	mA

Table 45: SC200L-EU Power Consumption

Description	Conditions	Min	Typ.
OFF state	Power down	TBD	μA

GSM/GPRS supply current	Sleep (USB disconnected) @ DRX = 2	TBD	mA
	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
GSM voice call	EGSM900 @ PCL 5	TBD	mA
	EGSM900 @ PCL 12	TBD	mA
	EGSM900 @ PCL 19	TBD	mA
	DCS1800 @ PCL 0	TBD	mA
	DCS1800 @ PCL 7	TBD	mA
	DCS1800 @ PCL 15	TBD	mA
WCDMA voice call	B1 @ max power	TBD	mA
	B5 @ max power	TBD	mA
	B8 @ max power	TBD	mA
GPRS data transfer	EGSM900 (1UL/4DL) @ PCL 5	TBD	mA

	EGSM900 (2UL/3DL) @ PCL 5	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 5	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 5	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 0	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 0	TBD	mA
	DCS1800 (3UL/2DL) @ PCL0	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 0	TBD	mA
EDGE data transfer	EGSM900 (1UL/4DL) @ PCL 8	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 8	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 8	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 8	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 2	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 2	TBD	mA
	DCS1800 (3UL/2DL) @ PCL 2	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 2	TBD	mA
WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA
	B5 (HSDPA) @ max power	TBD	mA
	B8 (HSDPA) @ max power	TBD	mA
	B1 (HSUPA) @ max power	TBD	mA
	B5 (HSUPA) @ max power	TBD	mA
	B8 (HSUPA) @ max power	TBD	mA
LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
	LTE-FDD B3 @ max power	TBD	mA
	LTE-FDD B5 @ max power	TBD	mA
	LTE-FDD B7 @ max power	TBD	mA

	LTE-FDD B8 @ max power	TBD	mA
	LTE-FDD B20 @ max power	TBD	mA
	LTE-FDD B28(A + B) @ max power	TBD	mA
	LTE-TDD B38 @ max power	TBD	mA
	LTE-TDD B40 @ max power	TBD	mA
	LTE-TDD B41 @ max power	TBD	mA

Table 46: SC200L-AU* Power Consumption

Description	Conditions	Min	Typ.
OFF state	Power down	TBD	μA
GSM/GPRS supply current	Sleep (USB disconnected) @ DRX = 2	TBD	mA
	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA

GSM voice call	GSM850 @ PCL 5	TBD	mA
	GSM850 @ PCL 12	TBD	mA
	GSM850 @ PCL 19	TBD	mA
	EGSM900 @ PCL 5	TBD	mA
	EGSM900 @ PCL 12	TBD	mA
	EGSM900 @ PCL 19	TBD	mA
	DCS1800 @ PCL 0	TBD	mA
	DCS1800 @ PCL 7	TBD	mA
	DCS1800 @ PCL 15	TBD	mA
	PCS1900 @ PCL 0	TBD	mA
	PCS1900 @ PCL 7	TBD	mA
	PCS1900 @ PCL 15	TBD	mA
WCDMA voice call	B1 @ max power	TBD	mA
	B2 @ max power	TBD	mA
	B4 @ max power	TBD	mA
	B5 @ max power	TBD	mA
	B8 @ max power	TBD	mA
GPRS data transfer	GSM850 (1UL/4DL) @ PCL 5	TBD	mA
	GSM850 (2UL/3DL) @ PCL 5	TBD	mA
	GSM850 (3UL/2DL) @ PCL 5	TBD	mA
	GSM850 (4UL/1DL) @ PCL 5	TBD	mA
	EGSM900 (1UL/4DL) @ PCL 5	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 5	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 5	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 5	TBD	mA

	DCS1800 (1UL/4DL) @ PCL 0	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 0	TBD	mA
	DCS1800 (3UL/2DL) @ PCL0	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 0	TBD	mA
	PCS1900 (1UL/4DL) @ PCL 0	TBD	mA
	PCS1900 (2UL/3DL) @ PCL 0	TBD	mA
	PCS1900 (3UL/2DL) @ PCL 0	TBD	mA
	PCS1900 (4UL/1DL) @ PCL 0	TBD	mA
EDGE data transfer	GSM850 (1UL/4DL) @ PCL 8	TBD	mA
	GSM850 (2UL/3DL) @ PCL 8	TBD	mA
	GSM850 (3UL/2DL) @ PCL 8	TBD	mA
	GSM850 (4UL/1DL) @ PCL 8	TBD	mA
	EGSM900 (1UL/4DL) @ PCL 8	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 8	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 8	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 8	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 2	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 2	TBD	mA
	DCS1800 (3UL/2DL) @ PCL 2	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 2	TBD	mA
	PCS1900 (1UL/4DL) @ PCL 2	TBD	mA
	PCS1900 (2UL/3DL) @ PCL 2	TBD	mA
	PCS1900 (3UL/2DL) @ PCL 2	TBD	mA
	PCS1900 (4UL/1DL) @ PCL 2	TBD	mA
WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA

	B2 (HSDPA) @ max power	TBD	mA
	B4 (HSDPA) @ max power	TBD	mA
	B5 (HSDPA) @ max power	TBD	mA
	B8 (HSDPA) @ max power	TBD	mA
	B1 (HSUPA) @ max power	TBD	mA
	B2 (HSUPA) @ max power	TBD	mA
	B4 (HSUPA) @ max power	TBD	mA
	B5 (HSUPA) @ max power	TBD	mA
	B8 (HSUPA) @ max power	TBD	mA
LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
	LTE-FDD B2 @ max power	TBD	mA
	LTE-FDD B3 @ max power	TBD	mA
	LTE-FDD B4 @ max power	TBD	mA
	LTE-FDD B5 @ max power	TBD	mA
	LTE-FDD B7 @ max power	TBD	mA
	LTE-FDD B8 @ max power	TBD	mA
	LTE-FDD B28(A + B) @ max power	TBD	mA
	LTE-TDD B38 @ max power	TBD	mA

7.5. Tx Power

The following table shows the RF output power of the module.

Table 47: SC200L-CE* RF Output Power

Frequency Band	Max.	Min.
EGSM900	TBD	TBD

DCS1800	TBD	TBD
WCDMA B1	TBD	TBD
WCDMA B8	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B34	TBD	TBD
LTE-TDD B38	TBD	TBD
LTE-TDD B39	TBD	TBD
LTE-TDD B40	TBD	TBD
LTE-TDD B41	TBD	TBD

Table 48: SC200L-EU RF Output Power

Frequency	Max.	Min.
EGSM900	TBD	TBD
DCS1800	TBD	TBD
WCDMA B1	TBD	TBD
WCDMA B5	TBD	TBD
WCDMA B8	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B7	TBD	TBD
LTE-FDD B8	TBD	TBD

LTE-FDD B20	TBD	TBD
LTE-FDD B28(A + B)	TBD	TBD
LTE-TDD B38	TBD	TBD
LTE-TDD B40	TBD	TBD
LTE-TDD B41	TBD	TBD

Table 49: SC200L-AU* RF Output Power

Frequency	Max.	Min.
GSM850	TBD	TBD
EGSM900	TBD	TBD
DCS1800	TBD	TBD
PCS1900	TBD	TBD
WCDMA B1	TBD	TBD
WCDMA B2	TBD	TBD
WCDMA B4	TBD	TBD
WCDMA B5	TBD	TBD
WCDMA B8	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B2	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B4	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B7	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B28(A + B)	TBD	TBD

LTE-TDD B38	TBD	TBD

NOTE

In GPRS 4-slot TX mode, the maximum output power is reduced by 3 dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

7.6. Rx Sensitivity

The following table shows the conducted RF receiving sensitivity of the module.

Table 50: SC200L-CE* RF Receiving Sensitivity

Frequency Band	Primary	Diversity	SIMO	3GPP (SIMO)
EGSM900	TBD	-	-	-102.4 dBm
DCS1800	TBD	-	-	-102.4 dBm
WCDMA B1	TBD	TBD	TBD	-106.7 dBm
WCDMA B8	TBD	TBD	TBD	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm

Table 51: SC200L-EU RF Receiving Sensitivity

Frequency Band	Primary	Diversity	SIMO	3GPP (SIMO)
EGSM900	TBD	-	-	-102.4 dBm
DCS1800	TBD	-	-	-102.4 dBm
WCDMA B1	TBD	TBD	TBD	-106.7 dBm
WCDMA B5	TBD	TBD	TBD	-104.7 dBm
WCDMA B8	TBD	TBD	TBD	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm

Table 52: SC200L-AU* RF Receiving Sensitivity

Frequency Band	Primary	Diversity	SIMO	3GPP (SIMO)
GSM850	TBD	-	-	-102.4 dBm
EGSM900	TBD	-	-	-102.4 dBm
DCS1800	TBD	-	-	-102.4 dBm
PCS1900	TBD	-	-	-102.4 dBm
WCDMA B1	TBD	TBD	TBD	-106.7 dBm

WCDMA B2	TBD	TBD	TBD	-104.7 dBm
WCDMA B4	TBD	TBD	TBD	-106.7 dBm
WCDMA B5	TBD	TBD	TBD	-104.7 dBm
WCDMA B8	TBD	TBD	TBD	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3 dBm

7.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatic discharge characteristics of the module.

Table 53: ESD Characteristics (Temperature: 25 °C, Humidity: 45 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

8 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimension tolerances are ±0.2 mm unless otherwise specified.

8.1. Mechanical Dimensions

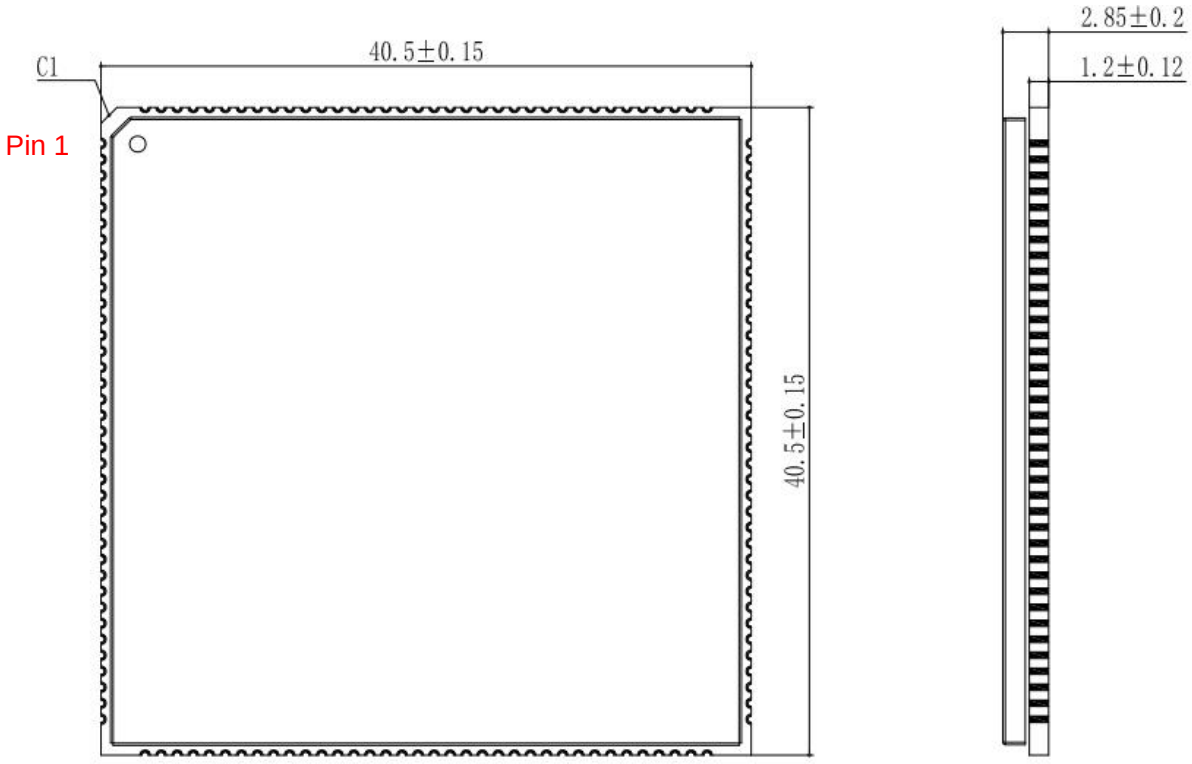


Figure 41: Module Top and Side Dimensions

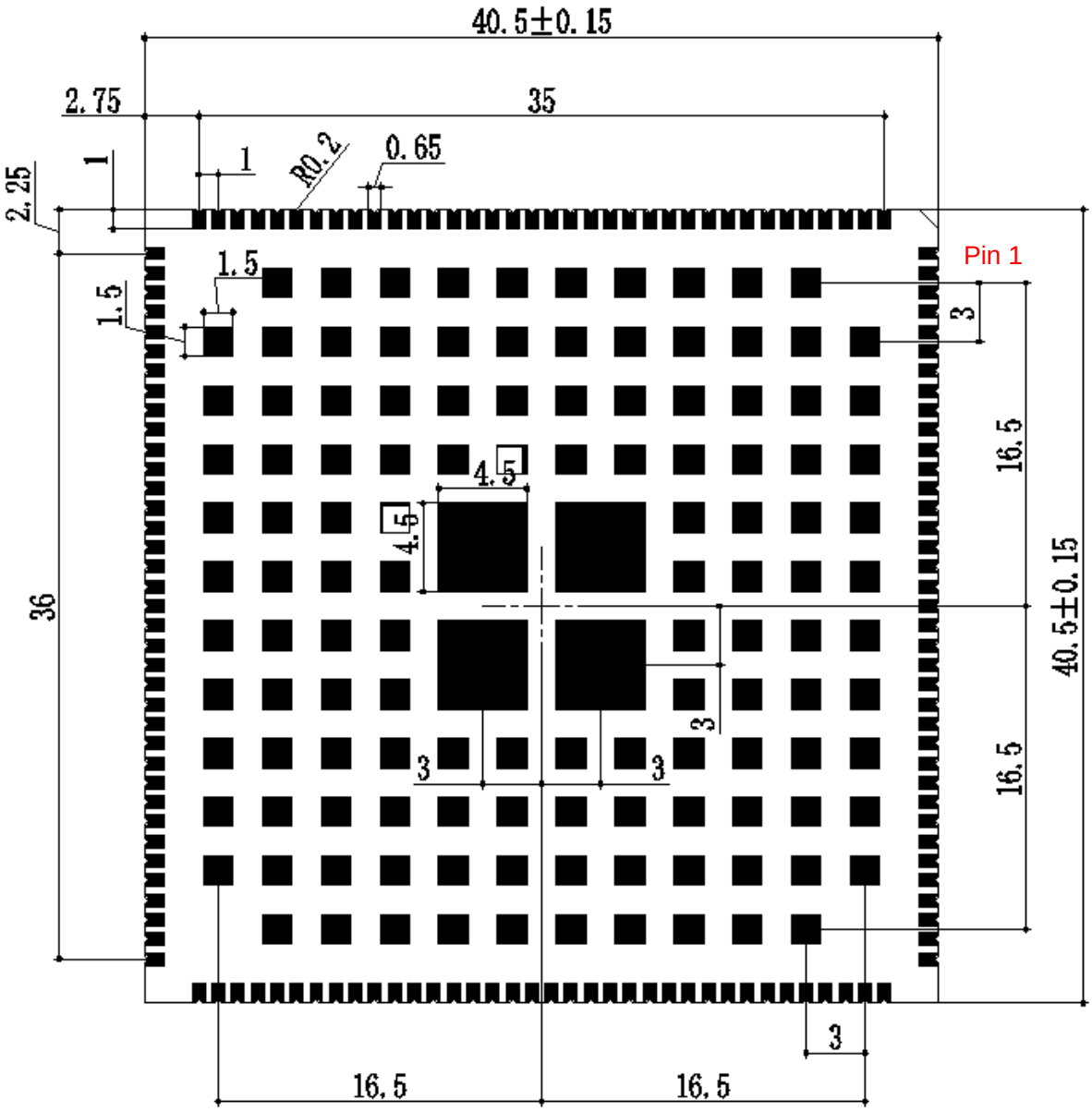


Figure 42: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to JEITA ED-7306 standard.

8.2. Recommended Footprint

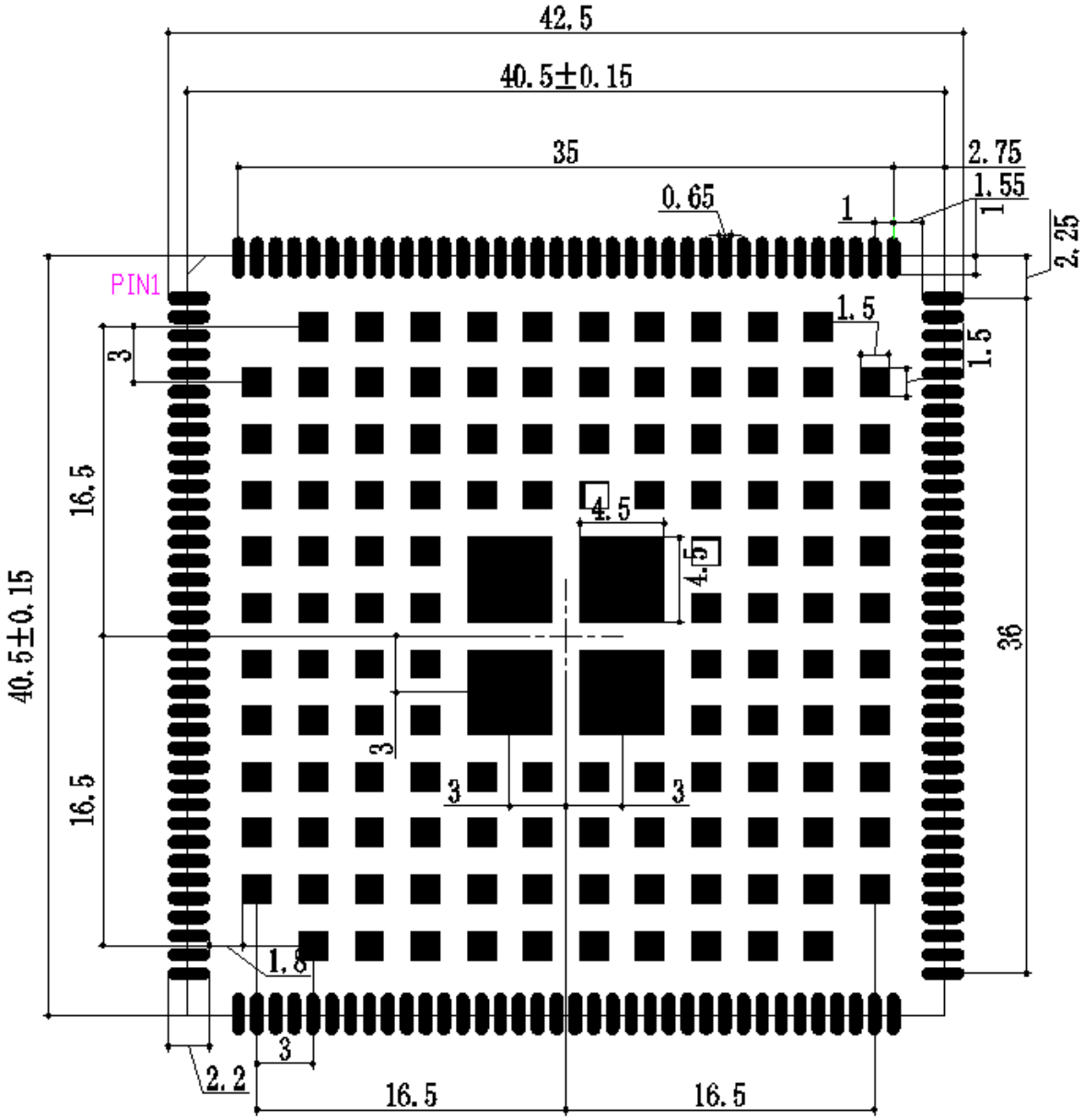


Figure 43: Recommended Footprint (Top View)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom Views

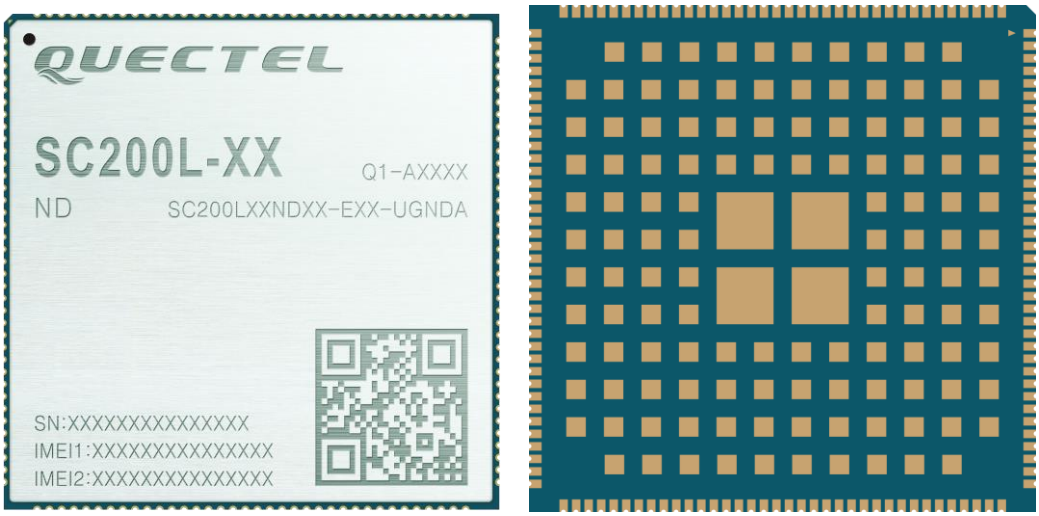


Figure 44: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [4] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[4] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [5]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

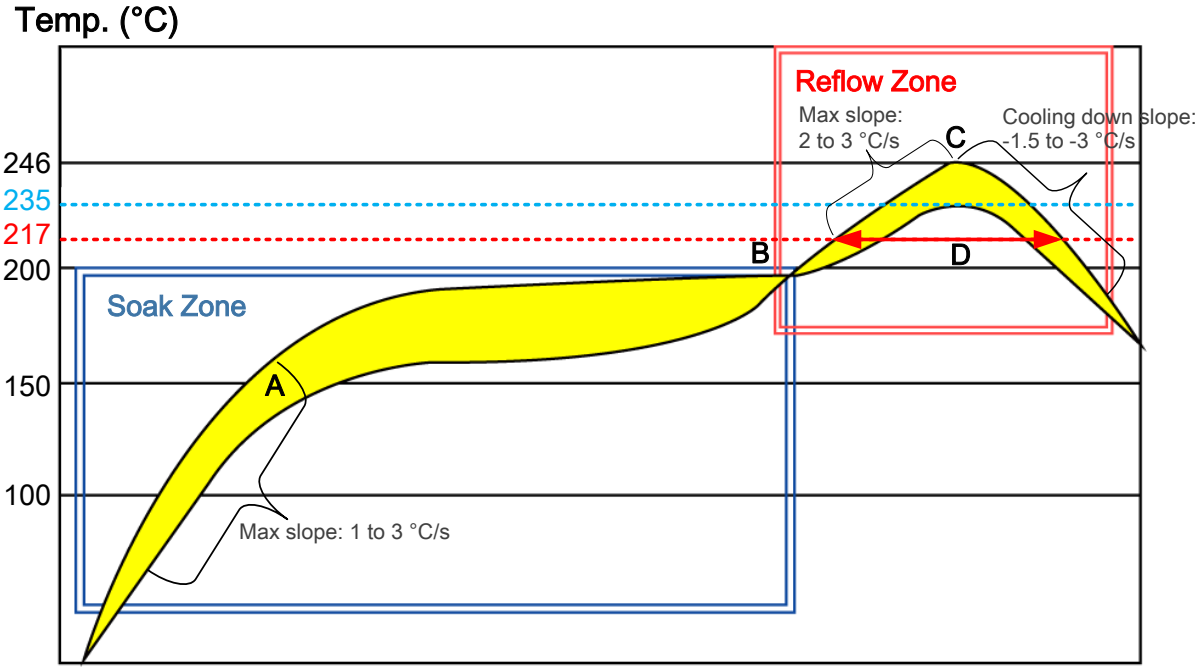


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 54: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

9.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follows:

9.3.1. Carrier Tape

Dimension details are as follows:

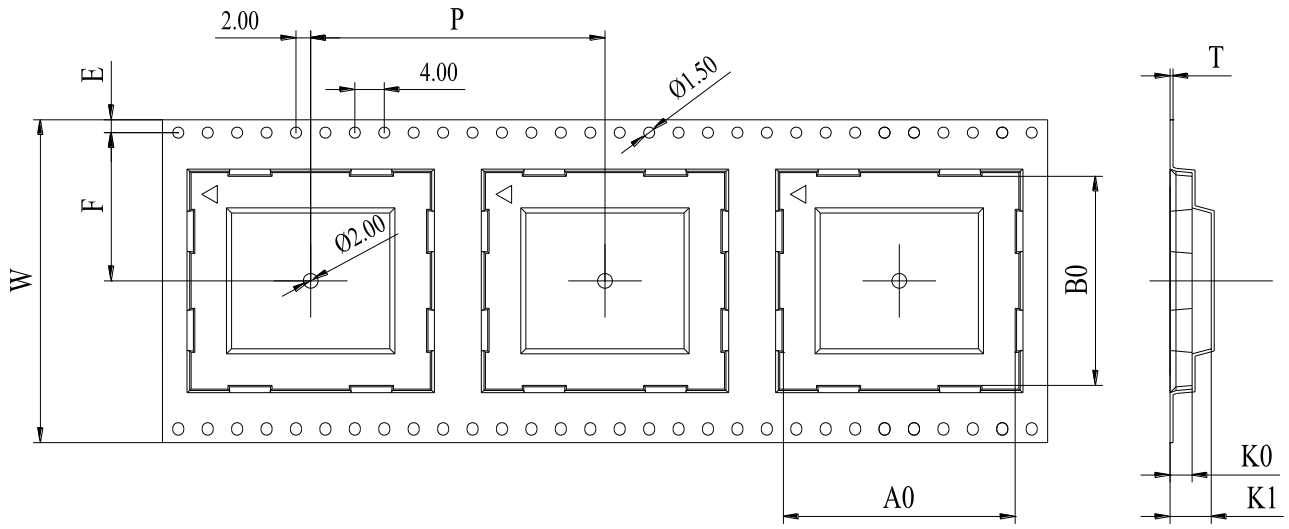


Figure 46: Carrier Tape Dimension Drawing

Table 55: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	41.2	41.2	4.0	4.6	34.2	1.75

9.3.2. Plastic Reel

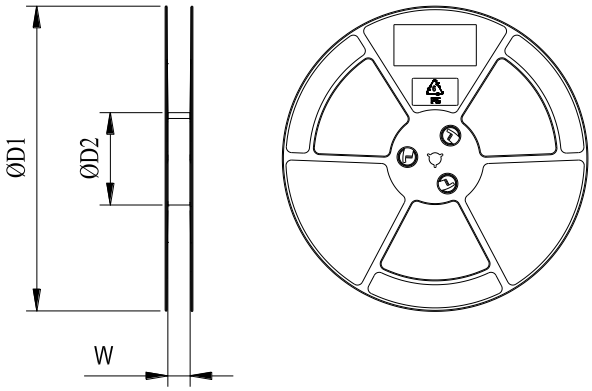
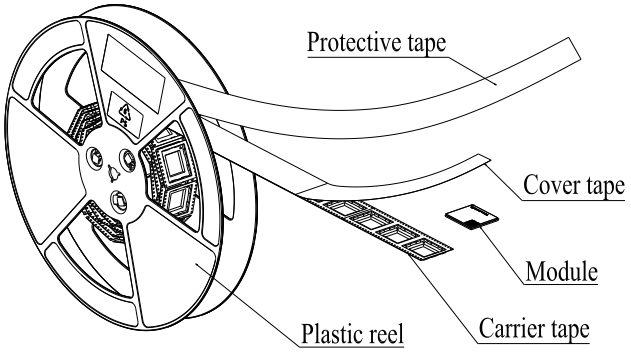


Figure 47: Plastic Reel Dimension Drawing

Table 56: Plastic Reel Dimension Table (Unit: mm)

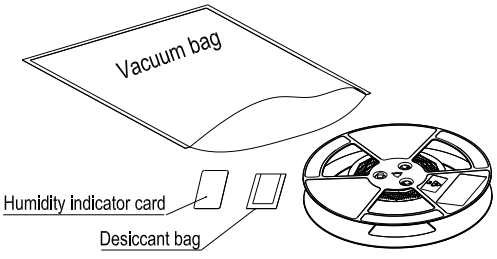
øD1	øD2	W
380	180	72.5

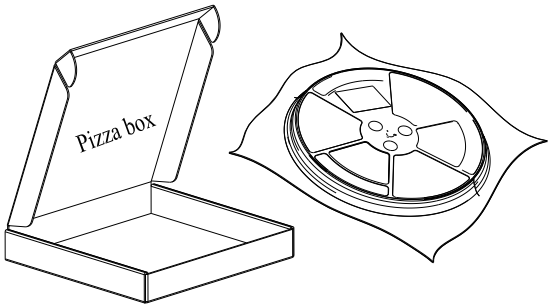
9.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 800 modules.

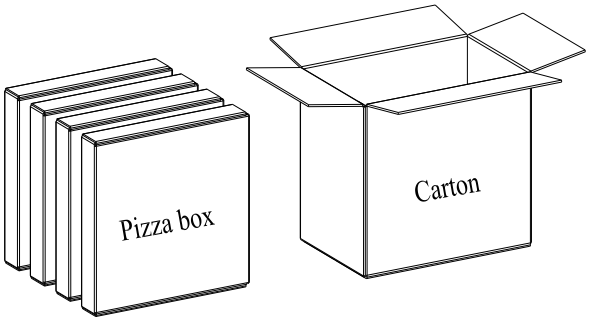


Figure 48: Packaging Process

10 Appendix References

Table 57: Related Documents

Document Name
[1] Quectel_Smart_EVB_G2_User_Guide
[2] Quectel_SC200L_Series(Dual-band_Wi-Fi)_Reference_Design
[3] Quectel_SC200L_Series(Dual-band_Wi-Fi)_Pin_Description_and_GPIO_Configuration
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Secondary_SMT_Application_Note

Table 58: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ALS	Ambient Light Sensor
AMR	Adaptive Multi-rate
AP	Access Point
ARM	Advanced RISC Machine
BB	Baseband
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
CEP	Circular Error Probable
CS	Coding Scheme

CSI	Camera Serial Interface
CTS	Clear to Send
DCS	Digital Cellular System
DL	Downlink
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
DRX	Discontinuous Reception
DSI	Display Serial Interface
ECM	Electret Condenser Microphone
EDGE	Enhanced Data Rate for GSM Evolution
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM
eMMC	Embedded Multimedia Card
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
fps	Frame per Second
FR	Full Rate
GFSK	Gaussian Frequency Shift Keying
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying

GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GRFC	Generic RF control
GSM	Global System for Mobile Communications
HD+	High Definition Plus
HR	Half Rate
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HT	High Throughput
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
I2C	Inter-Integrated Circuit
IMT-2000	International Mobile Telecommunications for the year 2000
$I_O$max	Maximum Output Load Current
IoT	Internet of Things
LCC	Leadless Chip Carrier
LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LE	Low Energy

LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low-Power Double Data Rate
LTE	Long-Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MEMS	Micro-Electro-Mechanical System
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSL	Moisture Sensitivity Levels
NTC	Negative Temperature Coefficient
OTA	Over-the-Air Upgrade
OTG	On-The-Go
OTP	One Time Programable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication Service
PDU	Protocol Data Unit
PHY	Physical Layer
PMU	Power Management Unit
POS	Point of Sale

PS	Proximity Sensor
PWM	Pulse Width Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
SAW	Surface Acoustic Wave
SCO	Synchronous Connection Oriented
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
STA	Station
TDD	Time-Division Duplex
TP	Touch Panel
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus

(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
WAPI	WLAN Authentication and Privacy Infrastructure
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network