EICUT-E70x

Hardware Design Manual

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Email: info@eicut.com

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Revision History

Date	Version	Description	Author
2025-10-06	1.0.0	Creation of the document	Sam

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1. Introduction

This document defines the **E70x Series module** and the air interface and hardware interfaces connecting it to customer applications.
It helps customers quickly understand the interface specifications, electrical characteristics, mechanical specifications, and related product information of the **E70x Series** module. With the assistance of this document, together with our application manuals and user guides, customers can rapidly deploy the **E70x Series** module in wireless applications.

The **E70x Series wireless module** is a broadband wireless terminal product supporting multiple network standards and frequency bands, including **TDD-LTE** and **FDD-LTE**.

Supported access data rates of the E70x Series:

TDD-LTE: 8 Mbps (downlink) / 2 Mbps (uplink)

FDD-LTE: 10 Mbps (downlink) / 5 Mbps (uplink)

The **E70x Series** provides wireless data access and is widely applicable in the **M2M** field, such as **OTT devices, CPE, routers, data cards, tablet computers, security systems, and industrial-grade PDAs**.

1.1. Safety Precautions

By following the safety principles below, personal safety can be ensured and potential damage to products and the working environment can be avoided:

Table 1- List of safety principles

	Driving safety first! When you are driving, do not use a handheld mobile terminal unless it has a hands-free function. Please stop and call again!
	Please turn off the mobile terminal device before boarding. The wireless function of the mobile terminal must not be turned on on the airplane to prevent interference to the communication system of the airplane. Ignoring this prompt may lead to flight safety and even violate the law.
	In hospitals or health care facilities, pay attention to whether there are restrictions on the use of mobile terminal equipment. RF interference can cause medical equipment to malfunction, so mobile terminal equipment may need to be turned off.
	The mobile terminal device cannot be effectively connected under any circumstances, and there is no call charge on the mobile device or the SIM is invalid. When you encounter the above situations in an emergency, please remember to make an emergency call and ensure that your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device receives and transmits radio frequency signals when it is turned on. Radio frequency interference occurs when it is close to TVs, radio computers or other electronic equipment.
	Keep mobile devices away from flammable gases. When you are close to a gas station, oil depot, chemical plant or explosion site, please turn off the mobile terminal device. There are potential safety hazards in operating electronic equipment in any potentially explosive place.

1.2. Document Purpose

This document provides a detailed description of the basic functions, key features, hardware interfaces and their usage, structural characteristics, power consumption specifications, and electrical characteristics of the **E70x Series** wireless module.
It is intended to guide users in integrating the **E70x Series** module into the design of various application terminals.

1.3. Contents Overview

This document is organized as follows:

- **Chapter 1:** Safety precautions, document purpose, revision history, etc.
- **Chapter 2:** Basic functions and key features of the **E70x Series** wireless module.
- **Chapter 3:** Detailed description of the functions, characteristics, and usage of each hardware interface of the **E70x Series**.
- **Chapter 4:** Antenna interface details and related precautions.
- **Chapter 5:** Detailed electrical characteristics of the **E70x Series**.
- **Chapter 6:** Structural characteristics of the **E70x Series** and related considerations.
- **Chapter 7:** Storage and production considerations for the **E70x Series**.
- **Chapter 8:** Appendix A – Reference documents and terminology abbreviations.

2. Product Overview

2.1. General Description

The **E70x Series** is a wireless communication module supporting **TDD-LTE** and **FDD-LTE**.
It supports TDD-LTE and FDD-LTE network data connections and also provides services such as **SMS**.
It supports **Wi-Fi Scan positioning** (China version only) and **GPS / BDS / GLONASS / Galileo / QZSS**.

Table 2-Supported frequency bands of the E70x Series module

Item	Description
TDD-LTE	**B34/B38/B39/B40/B41**
FDD-LTE	**B1/B3/B5/B8**

The **E70x Series** adopts an advanced highly integrated design, integrating RF and baseband on a single PCB to complete wireless reception, transmission, and baseband signal processing.
A single-sided layout is used. The module dimensions are **15.8 × 17.7 × 2.4 mm**.

2.2. Key Performance

The table below describes the main performance characteristics of the **E70x Series** module.

Table 3- Main Module Features

Parameter	Description
Power Supply	- VBAT supply voltage range: 3.5 V – 4.2 V- Typical supply voltage: 3.8 V
Transmit Power	- Class 3 (23 dBm ±2.7 dB) for FDD-LTE bands - Class 3 (23 dBm ±2.7 dB) for TDD-LTE bands
LTE Features	- Maximum support: CAT1 Bis - RF bandwidth: 1.4–20 MHz - FDD: Max uplink 5 Mbps, max downlink 10 Mbps - TDD: Max uplink 2 Mbps, max downlink 8 Mbps
Positioning	- Supports Wi-Fi Scan positioning, sharing the main antenna

Network Protocols	- TCP / UDP / MQTT / FTP / FTPS / HTTP / HTTPS / LWM2M / CoAP
USIM Card Interface	- Supports USIM/SIM cards: 1.8 V and 3 V
PCM Interface	- Used for audio applications; requires external codec - Supports 16-bit linear encoding - Supports short-frame mode: module operates as master only
LCD Interface	- Supports SPI_LCD- Resolution: 240 × 320
I²C Interface	- Supports two I²C interfaces
USB Interface	- Supports USB 2.0- For AT commands, data transfer, software debugging and firmware upgrade- USB driver support: Windows 7 / 8 / 8.1 / 10
UART Interfaces	- **Main UART:** for AT commands and data transfer, default baud 115200 bps, supports RTS/CTS flow control - **Debug UART:** for debugging and log output, not general-purpose
AT Commands	- Compliant with 3GPP TS 27.007 and 27.005 - Additional EICUT proprietary AT commands
Network Status	- NET_STATUS pin indicates network status
Antenna Interfaces	- Main antenna (ANT_MAIN) / Wi-Fi Scan antenna (ANT_MAIN) - GNSS antenna (ANT_GNSS)
Physical Characteristics	- Dimensions: 15.8 × 17.7 × 2.4 mm
Temperature Range	- Operating: –35 °C to +75 °C - Storage: –40 °C to +85 °C
Software Upgrade	- Via USB interface
RoHS Compliance	- Fully compliant with EU RoHS
Environmental Humidity	- 5% – 95%
Functional Interfaces	- Power interface- USB 2.0 High-Speed interface - USIM/SIM card interface (3 V / 1.8 V) - Hardware reset interface - LED indicator interface - ADC interface- UART interface - PCM interface (optional) - LCM interface - I2C interface - USB_BOOT interface
Supported LTE Bands	- **TDD-LTE:** B34 / B38 / B39 / B40 / B41 - **FDD-LTE:** B1 / B3 / B5 / B8

2.3. Functional Block Diagram

The following diagram illustrates the main functional blocks of the **E70x Series module**:

Functional Unit

- Baseband Unit
- RF Unit
- Power Management Unit
- Peripheral Interfaces

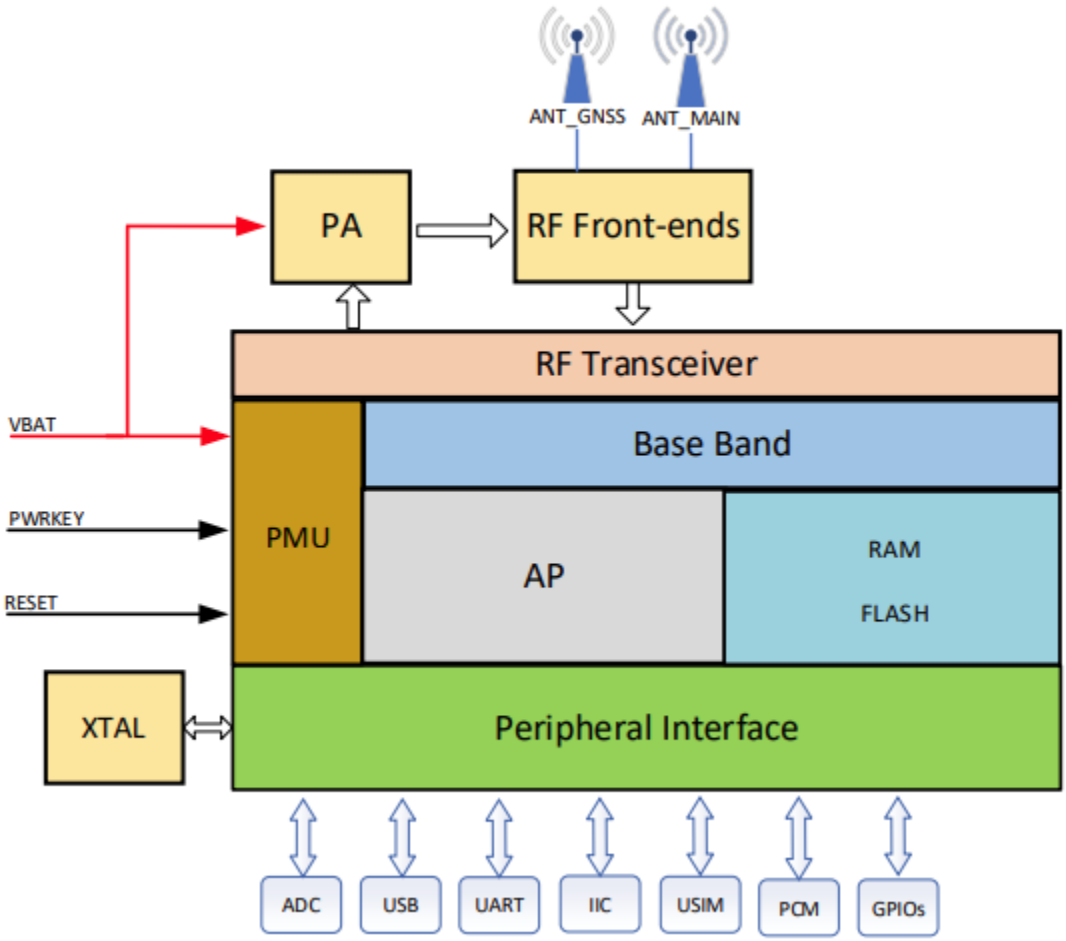

Figure 1-Functional Block Diagram

2.4. Evaluation Board

To facilitate testing and usage of the **E70x Series** module, the company provides an **evaluation board kit**.
The evaluation board includes:

- USB data cable
- Antenna
- Other peripheral components

3. Application Interfaces

3.1. General Description

The **E70x Series** uses **109 LGA pins**, providing the following functional interfaces:

Table 4-Interfaces

Interface	Description
Power Interface	Supplies power to the module
USB 2.0 High-Speed Interface	For AT commands, data transfer, debugging, and firmware upgrade
USIM/SIM Card Interface	Supports **3 V and 1.8 V** cards
Hardware Reset Interface	Allows hardware reset of the module
LED Indicator Interface	Status indication via LEDs
ADC Interface	Analog-to-digital conversion input
UART Interface	Serial communication interface
PCM Interface	Optional; used for audio applications
I²C Interface	For connecting peripherals
LCD Interface	Supports SPI_LCD interface
USB_BOOT Interface	For firmware programming / boot operations

3.2. LGA Interface Definition

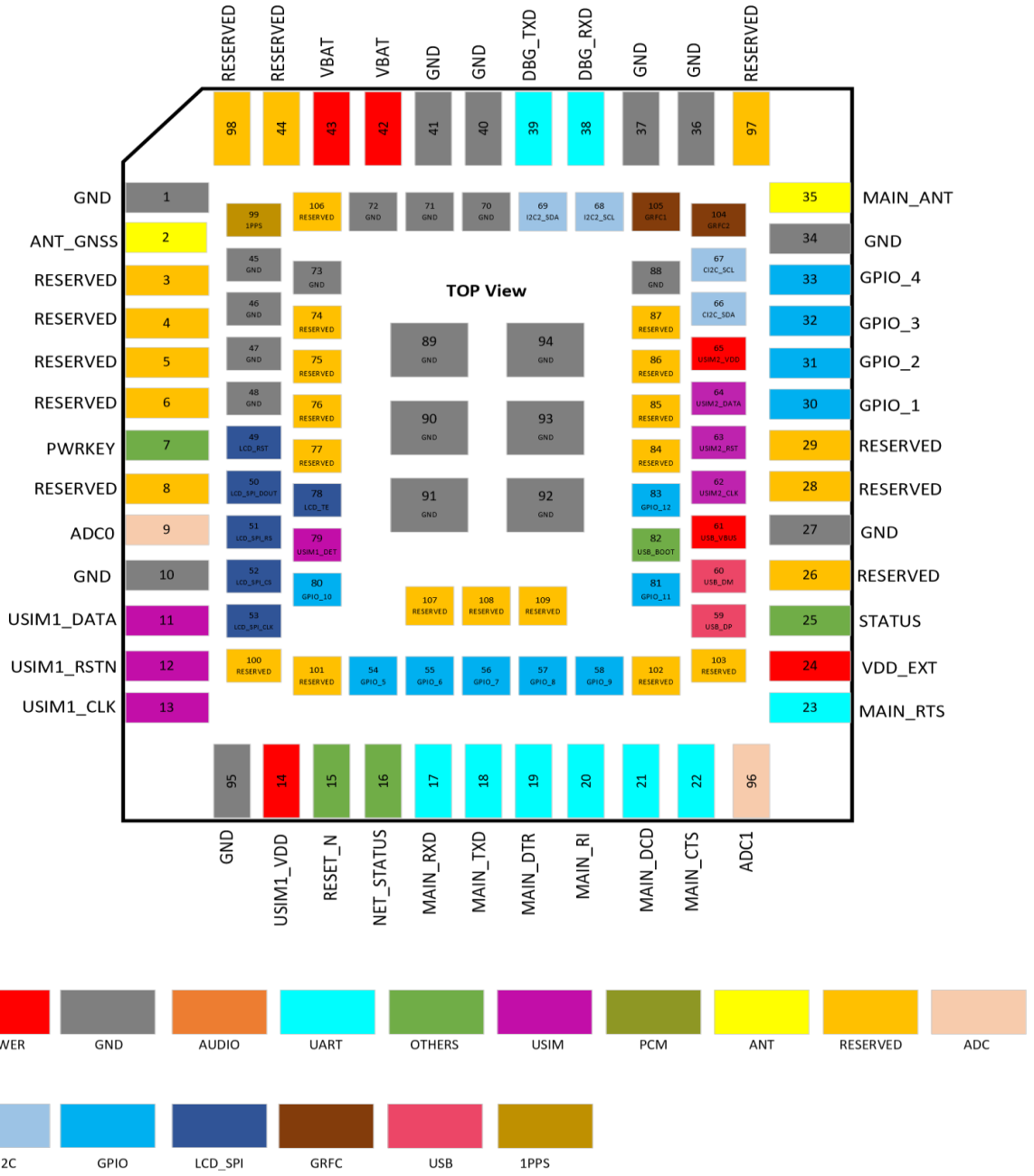

Figure 2-Module Pin Assignment Diagram (Top View)

3.3. Pin Type Description

The table below defines the I/O parameter types used by the **E70x Series** module.

Table 5- I/O Parameter Definition

Type	Description
I/O	Bidirectional digital signal
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
OD	Open-drain output
PI	Power input
PO	Power output

Table 6-Pin Description

Pin No.	Pin Name	Type	Level	Description	Remarks
1	GND	—	—	Ground	—
2	ANT_GNSS	AI	—	GNSS antenna interface	—
3–6	RESERVED	—	—	Reserved	—
7	PWRKEY	DI	VIL=0 V VIH=VBAT	Module power on/off control	Active low; default high after power-on
8	RESERVED	—	—	Reserved	—
9	ADC0	AI	0–1.2 V	ADC input	Series 1 kΩ required; leave floating if unused
10	GND	—	—	Ground	—
11	USIM1_DATA	DI/O	1.8 V / 3.0 V	SIM1 data signal	—
12	USIM1_RST	DO	1.8 V / 3.0 V	SIM1 reset signal	—
13	USIM1_CLK	DO	1.8 V / 3.0 V	SIM1 clock signal	—

14	USIM1_VDD	PO	1.8 V / 3.0 V	SIM1 power supply	—
15	RESET_N	DI	VIL=0 V VIH=1.8 V	Module reset	Active low
16	NET_STATUS	DO	0 / 1.8 V	Network status indicator	Leave floating if unused
17	MAIN_RXD	DI	0 / 1.8 V	Main UART receive	Used for AT commands
18	MAIN_TXD	DO	0 / 1.8 V	Main UART transmit	Used for AT commands
19	MAIN_DTR	DI	0 / 1.8 V	DTE ready signal	—
20	MAIN_RI	DO	0 / 1.8 V	Ring indicator	—
21	MAIN_DCD	DO	0 / 1.8 V	Carrier detect output	—
22	MAIN_CTS	DO	0 / 1.8 V	Clear to send	—
23	MAIN_RTS	DI	0 / 1.8 V	Request to send	—
24	VDD_EXT	PO	1.8 V	Digital level output (50 mA max)	Leave floating if unused
25	STATUS	DO	0 / 1.8 V	Module running status	—
26	RESERVED	—	—	Reserved	—
27	GND	—	—	Ground	—
28–29	RESERVED	—	—	Reserved	—
30	GPIO_1 / PCM_CLK	I/O	0 / 1.8 V	GPIO or PCM clock	Default GPIO
31	GPIO_2 / PCM_SYNC	I/O	0 / 1.8 V	GPIO or PCM frame sync	—
32	GPIO_3 / PCM_DIN	I/O	0 / 1.8 V	GPIO or PCM data input	—
33	GPIO_4 / PCM_DOUT	I/O	0 / 1.8 V	GPIO or PCM data output	—
34	GND	—	—	Ground	—
35	ANT_MAIN	AI	—	Main antenna / Wi-Fi Scan	Shared antenna
36–37	GND	—	—	Ground	—
38	DEBUG_RXD	DI	0 / 1.8 V	Debug UART RX	—

39	DEBUG_TXD	DO	0 / 1.8 V	Debug UART TX	—
40–41	GND	—	—	Ground	—
42–43	VBAT	PI	3.5–4.2 V	Power input	≥2 A current capability; TVS recommended
44	NC	—	—	Not connected	—
45–48	GND	—	—	Ground	—
49	LCD_RST	DO	0 / 1.8 V	LCD reset signal	—
50	LCD_SPI_DOUT	DO	0 / 1.8 V	LCD data output	—
51	LCD_SPI_RS	DO	0 / 1.8 V	LCD data/command select	—
52	LCD_SPI_CS	DO	0 / 1.8 V	LCD chip select	—
53	LCD_SPI_CLK	DO	0 / 1.8 V	LCD SPI clock	—
54–58	GPIO_5–GPIO_9	I/O	0 / 1.8 V	General GPIOs	GPIO_8 outputs high at startup
59	USB_DP	I/O	USB	USB DP signal	—
60	USB_DM	I/O	USB	USB DM signal	—
61	USB_VBUS	AI	3.5–5.0 V	USB insertion detection	—
62–65	USIM2_*	DO/DI/PO	1.8 V	SIM2 interface	SIM2 supports 1.8 V only
66–69	I2C / CI2C	OD	0 / 1.8 V	I²C interfaces	—
70–73	GND	—	—	Ground	—
74–77	RESERVED	—	—	Reserved	—
78	LCD_TE	DO	0 / 1.8 V	LCD frame sync	—
79	USIM1_DET	DI	0 / 1.8 V	SIM1 hot-plug detect	—
80–83	GPIO_10–GPIO_12	I/O	0 / 1.8 V	General GPIOs	—
84–87	RESERVED	—	—	Reserved	—
88–95	GND	—	—	Ground	—
96	ADC1	AI	0–1.2 V	ADC input	Series 1 kΩ required
97–98	RESERVED	—	—	Reserved	—

99	1PPS	DO	0 / 1.8 V	GNSS 1PPS output	Do not pull low
100–103	RESERVED	—	—	Reserved	—
104	GRFC2	DO	0 / 1.8 V	RF control GPIO	—
105	GRFC1	DO	0 / 1.8 V	RF control GPIO	—
106–109	RESERVED	—	—	Reserved	—

Notes

1. Not all interfaces are supported simultaneously.
2. Some pins are multiplexed; please consider this carefully during hardware design.

3.4. Power Supply

Table 7-E70x Series Module Power Interface Description

Pin Name	I/O	Pin	Description
VBAT	PI	42, 43	Module power supply, 3.5–4.2 V, nominal value 3.8 V
VDD_EXT	PO	24	1.8 V output, 50 mA load capability

3.4.1. Power Supply

The **E70x Series** module needs to be powered through the VBAT pin. The recommended power supply design is shown in Figure 3.

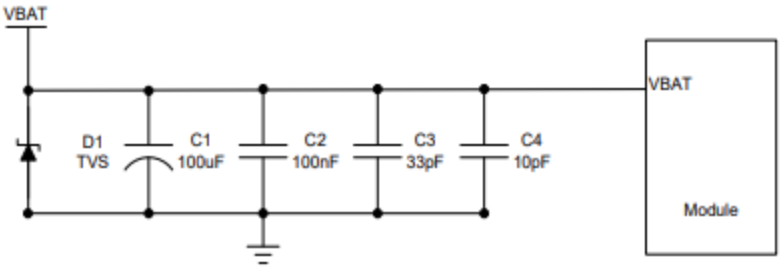

Figure 3-Module Power Supply Circuit

To reduce voltage drop, a 100 µF low-ESR filter capacitor must be used. Chip multilayer ceramic capacitors (MLCC) have the best ESR performance. It is recommended to add three ceramic capacitors (100 nF, 33 pF, 10 pF) to the VBAT pin, and the capacitors must be placed close to the VBAT pin.

At the same time, in order to ensure better power supply performance, a TVS diode should be added near the module VBAT input to improve the module's electrostatic discharge tolerance. When an external power supply is connected to the module, VBAT must use star routing. The VBAT trace width should not be less than 1.5 mm. In principle, the longer the VBAT trace, the wider the trace should be.

3.4.2. Reducing Voltage Drop

The power supply range of the **E70x Series** is 3.5 V to 4.2 V. During data transmission or calls, instantaneous high-power transmission can generate current peaks of up to 1.5 A, which can cause large ripple on VBAT. If an instantaneous voltage drop causes the VBAT supply voltage to be too low, the module will restart or shut down.

To ensure normal operation of the module, the power supply must have sufficient current capability, and the input voltage must not be lower than 3.5 V.

Figure 4 below shows the voltage drop during burst transmission under a 4G network.

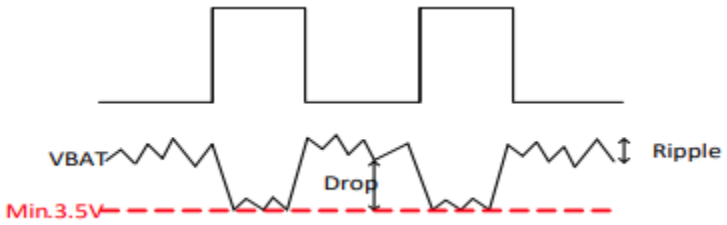

Figure 4-Burst Transmission Power Requirements

3.4.3. Power Supply Reference Circuit

The design of the module power supply is very important, because a large part of the module performance depends on the power supply. The **E70x Series** must use a power supply capable of providing at least 1.5 A current.

If the voltage difference between the input voltage and the module supply voltage is not large, it is recommended to use an LDO as the power supply. If there is a relatively large voltage difference between input and output, it is recommended to use a DCDC converter as the module power supply.

The figure below shows a reference design for a +5 V power supply circuit. This design uses an LDO from Micrel, model MIC29302WU. Its typical output voltage is 3.9 V, and the peak load current reaches 3 A.

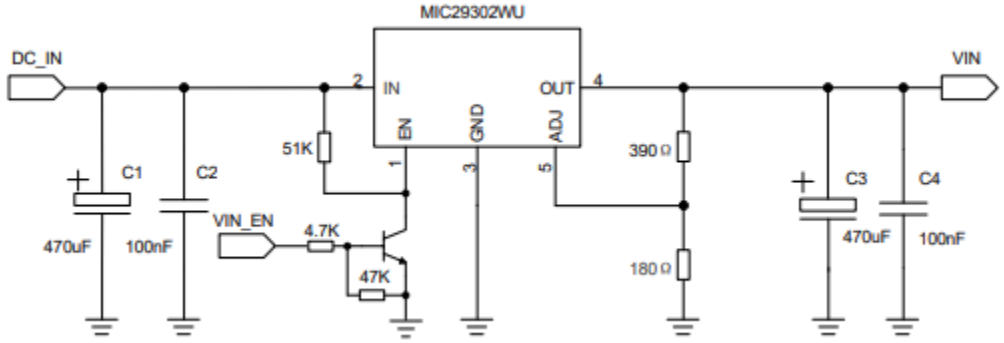

Figure 5-Power Input Reference Design

3.4.4. VDD_EXT Voltage Output

When the **E70x Series** module is powered on normally, there is a voltage output on Pin 24. The default output voltage is 1.8 V, with a current load of 50 mA. This output voltage can be used as an external pull-up source, such as a logic level reference, and the logic level status of this pin can also be read to determine whether the module is powered on.

3.5. Power On / Power Off

3.5.1. PWRKEY Pin Power-On

Table 8-PWRKEY Pin Power-On

Pin Name	I/O	Pin	Description

PWRKEY	DI	7	Power on/off signal

When the system is in the powered-off state and detects that PWRKEY is pulled low for more than 2 seconds, the chip powers on internally and enters the power-on process. The reference circuit is as follows:

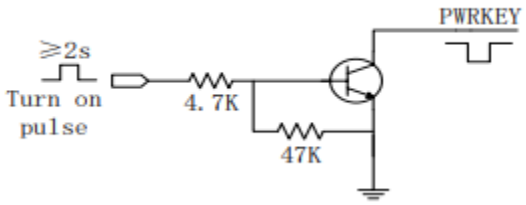

Figure 6-Driver-Based Power-On Reference Circuit

Another way to control the PWRKEY pin is directly through a push-button switch. A TVS must be placed near the button for ESD protection. The reference circuit is as follows:

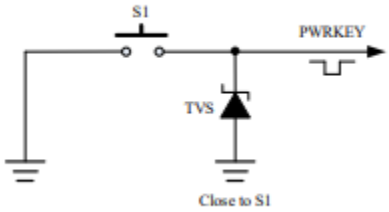

Figure 7-Key-Based Power-On Reference Circuit

The power-on timing is shown in the figure below:

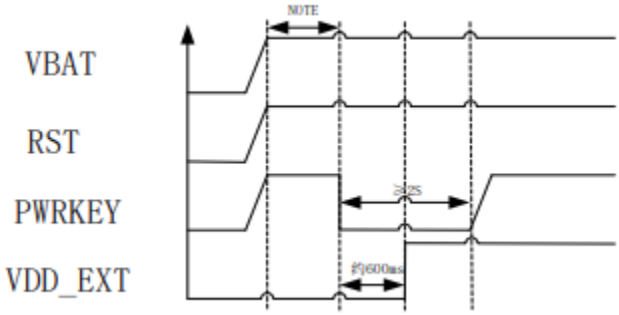

Figure 8-Power-On Timing Diagram

Note:
Before pulling PWRKEY low, it must be ensured that the VBAT voltage is stable.

3.5.2. Power-Off

Module power-off methods:

Table 9-Module power-off

Power-Off Method	Power-Off Method	Applicable Scenario
Low-voltage power-off	When the VBAT voltage is too low or power is lost, the module will power off	In this case, the module does not perform a normal power-off process and does not go through the process of deregistering from the base station
Hardware power-off	Pull PWRKEY low (greater than 3 s), then release	Normal power-off
AT power-off	AT command	Software power-off

Notes:

1. When the module is operating normally, do not immediately cut off the module power to avoid damaging the internal Flash data of the module. It is recommended to first shut down the module using AT commands, and then disconnect the power.
2. When using AT commands to power off, ensure that PWRKEY remains at a high level after the power-off command is executed. Otherwise, after the module completes the power-off process, it will automatically power on again.

The power-off timing is as follows:

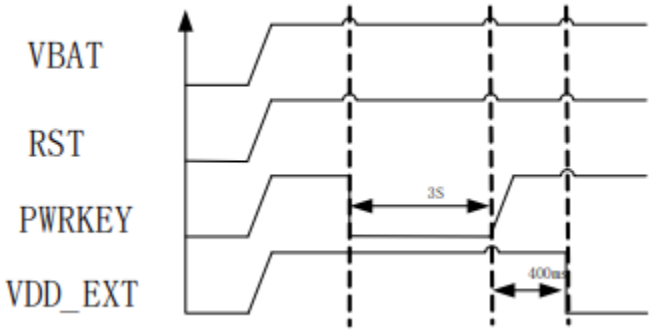

Figure 9-Power-Off Timing Diagram

3.6. Reset Function

Table 10-Reset Function

Pin Name	I/O	Pin	Pin Description
RESET_N	DI	15	Reset signal

The **E70x Series** has two reset methods: hardware reset and AT command reset. When the module is working, the software method uses AT commands to reset. The hardware reset method pulls the RESET_N pin low for at least 150 ms and then releases it to reset the module.

The RESET_N signal is relatively sensitive to interference; therefore, it is recommended that the routing on the module interface board be as short as possible and that ground shielding be applied.

The reference circuit is similar to the PWRKEY control circuit. Customers can use a driver circuit or a button to control the RESET_N pin.

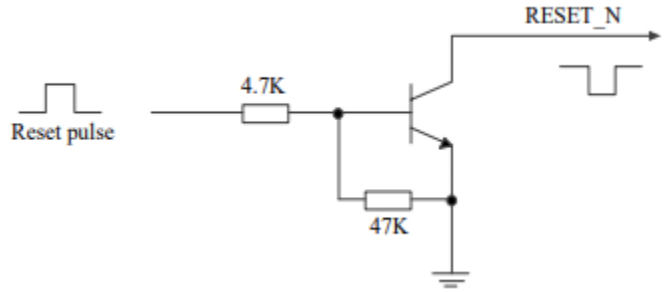

Figure 10-Driver-Based Reset Reference Circuit

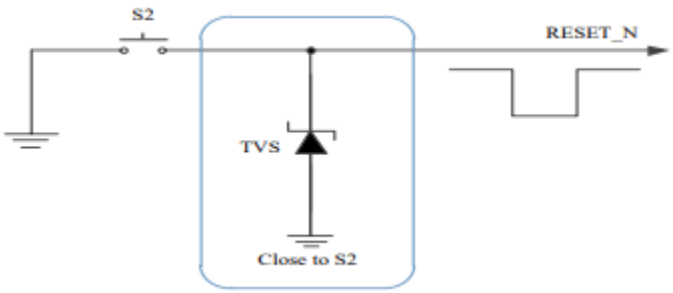

Figure 11-Key-Based Reset Reference Circuit

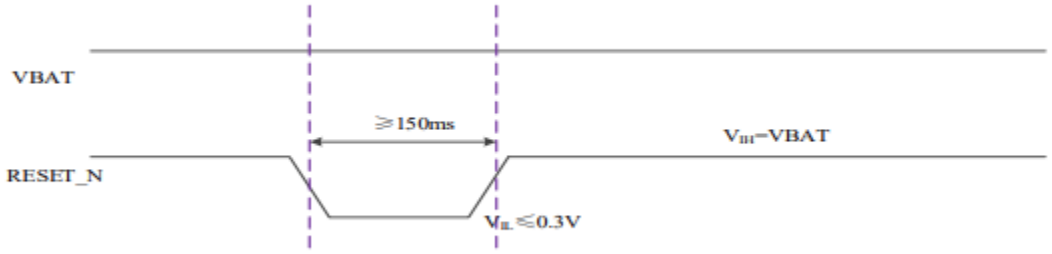

Figure 12-RESET_N Reset Timing Diagram

3.7. USIM Interface

The **E70x Series** supports 1.8 V and 3.0 V SIM cards. SIM1 supports 1.8 V and 3.0 V, while SIM2 only supports 1.8 V.

Table 11- USIM Interface Description

Pin Name	I/O	Pin	Pin Description
USIM1_DATA	DIO	11	SIM1 card data signal line
USIM1_RST	DO	12	SIM1 card reset signal line
USIM1_CLK	DO	13	SIM1 card clock signal line
USIM1_VDD	PO	14	SIM1 card power supply
USIM1_DET	DI	79	USIM1 card hot-plug detection signal
USIM2_CLK	DO	62	SIM2 card clock signal line
USIM2_RST	DO	63	SIM2 card reset signal line
USIM2_DATA	DIO	64	SIM2 card data signal line

USIM2_VDD	**PO**	**65**	**SIM2 card power supply**

The **E70x Series** module supports USIM card hot-plug functionality through the USIM1_DET pin. After a SIM card is inserted into the card holder shown in the figure, the SIM_DET pin is at a low level. When the SIM_DET pin level is high, no card is detected. Whether the SIM card hot-plug function is enabled can be configured through AT commands. It is enabled by default, and card detection is active low.

The SIM card circuit design with hot-plug functionality is shown in the figure below:

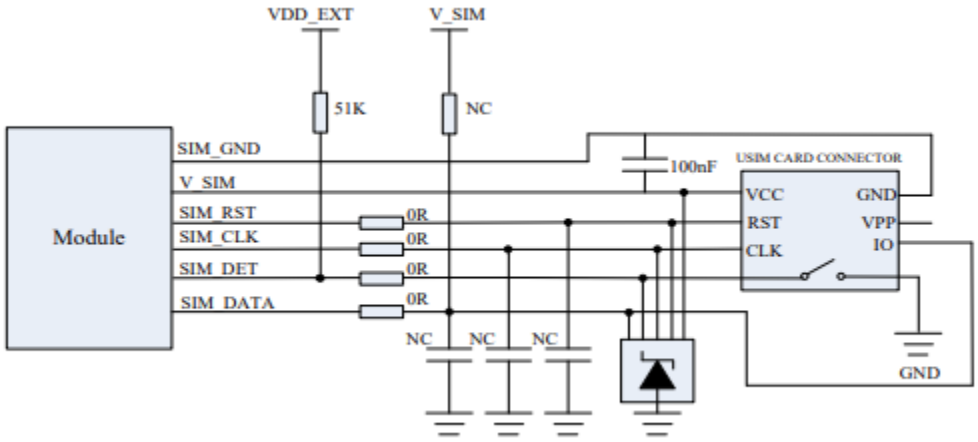

Figure 13-SIM Card Holder Reference Design with Hot-Plug Support

If SIM card hot-plug detection is not required, the USIM1_DET pin can be left floating. The reference circuit is shown below:

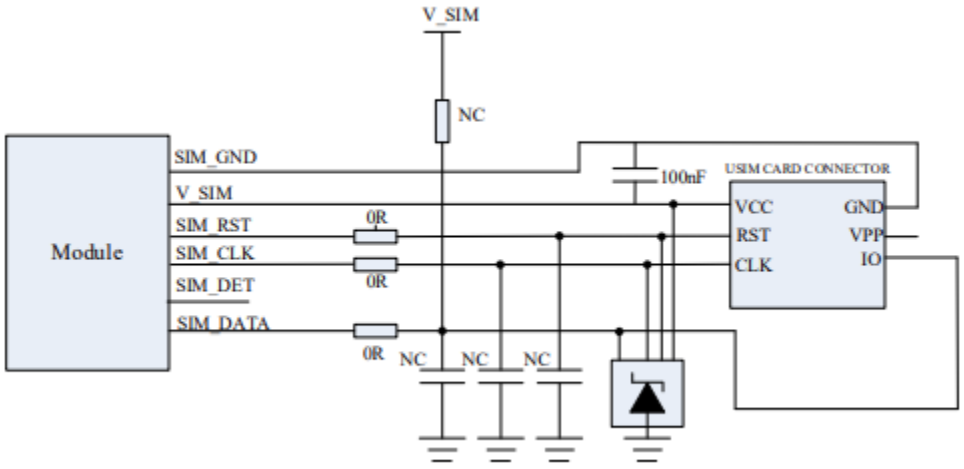

Figure 14-SIM Card Holder Reference Design without Hot-Plug Support

In the circuit design of the USIM card interface, in order to ensure good SIM card performance and reliability, it is recommended to follow the design principles below:

- Reserve a 0 Ω resistor on the SIM_DATA, SIM_CLK, and SIM_RST lines to facilitate debugging;
- To improve ESD immunity, add ESD protection devices with low parasitic capacitance on the SIM_VDD, SIM_DATA, SIM_CLK, and SIM_RST lines;
- Peripheral components of the SIM card should be placed as close as possible to the SIM card holder;
- The SIM card holder should be placed close to the module, and the SIM card signal routing length should be kept within 100 mm as much as possible;
- SIM card signal routing should be kept away from RF lines and VBAT power lines;
- To prevent crosstalk between the SIM_CLK signal and SIM_DATA, the two routings should not be too close, and ground shielding should be added between the two traces.

3.8. USB Interface

The **E70x Series** provides a USB interface compliant with the USB 2.0 specification. This interface is used for AT command interaction, data transmission, software debugging, and firmware upgrade.

3.8.1. USB Pin Description

The **E70x Series** module provides one USB 2.0 interface.

Table 12- USB Interface Description

Pin Name	I/O	Pin	Description
USB_DP	I/O	59	USB differential data +
USB_DM	I/O	60	USB differential data −
USB_VBUS	AI	61	USB insertion detection

3.8.2. USB Reference Circuit

The application reference circuit for the **E70x Series** module USB interface is shown in the figure below.

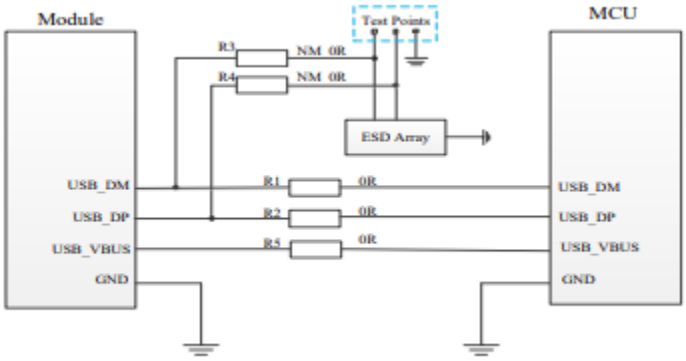

Figure 15-USB Interface Reference Design

To meet USB data line signal integrity requirements, resistors R1/R2/R3/R4 must be placed close to the module, and the resistors must be placed close to each other. The branch connecting to the test points must be as short as possible. In the USB interface circuit design, in order to ensure USB performance, it is recommended to follow the principles below:

- To reduce signal interference during high-speed USB data transmission, series resistors R1 and R2 can be added to the USB_DM and USB_DP interface circuits to improve data transmission accuracy. Both R1 and R2 are recommended to be 0 Ω;
- To improve ESD performance of the USB interface, it is recommended to add ESD protection devices on the USB_DP and USB_DM interface circuits. ESD devices with junction capacitance less than 1 pF are recommended. USB ESD protection devices should be placed as close as possible to the USB connector;
- To ensure reliable USB operation, more protection measures should be considered during design, such as layout protection. Impedance control of 90 Ω is required for USB_DP and USB_DM, routing must strictly follow differential requirements, and traces should be kept as far away as possible from interference signals;
- Do not route USB traces under crystal oscillators, oscillators, magnetic components, or RF signals. It is recommended to use inner-layer differential routing with ground shielding above, below, left, and right.

3.9. UART

The **E70x Series** module has two UARTs: the main UART (MAIN UART) and the debug UART (DEBUG UART). The main features of the main UART and debug UART are described below.

- The default baud rate of the main UART is 115200 bps, used for downloading and AT commands.
- The debug UART is used only for debugging and log output; it is not a general-purpose UART.

Table 13- Main UART Pin Description

Pin Name	I/O	Pin	Description
MAIN_CTS	DO	22	DTE clear to send
MAIN_RTS	DI	23	DTE request to send
MAIN_TXD	DO	18	Module transmit data
MAIN_RXD	DI	17	Module receive data
MAIN_DTR	DI	19	DTE ready
MAIN_RI	DO	20	Output ring indicator
MAIN_DCD	DO	21	Module output carrier detect

Table 14- Debug UART Pin Description

Pin Name	I/O	Pin	Description
DEBUG_RXD	DI	38	DEBUG UART receive
DEBUG_TXD	DO	39	DEBUG UART transmit

Table 15- UART Logic Levels

Pin Name	I/O	Pin	Description
VIL	**-0.3**	**0.6**	**V**
VIH	**1.2**	**2.0**	**V**
VOL	**0**	**0.45**	**V**
VOH	**1.35**	**1.8**	**V**

The UART logic level of the **E70x Series** module is 1.8 V. If the customer host is 3.3 V, a level shifter must be added in the UART application. The figure below shows the reference design:

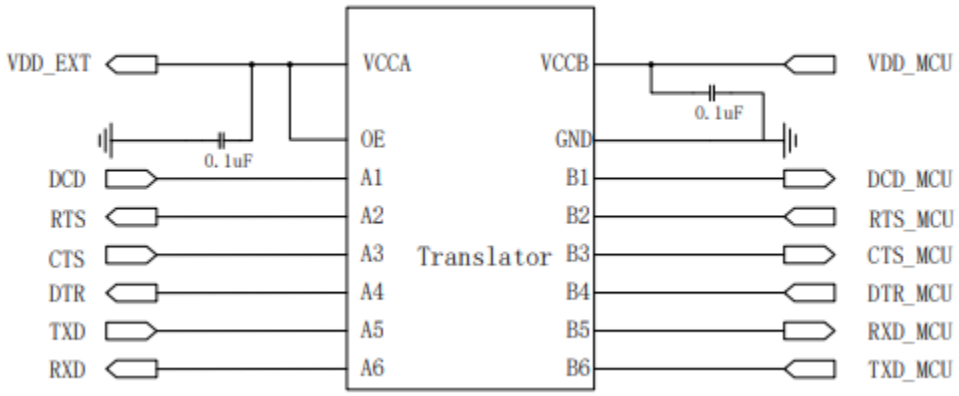

Figure 16-Level Shifter IC Reference Circuit

Another level-shifting circuit is shown in the figure below. The input and output circuit design of the dashed part can refer to the solid-line part, but attention must be paid to the connection direction. At the same time, this level-shifting circuit is not suitable for applications with baud rates higher than 460 Kbps.

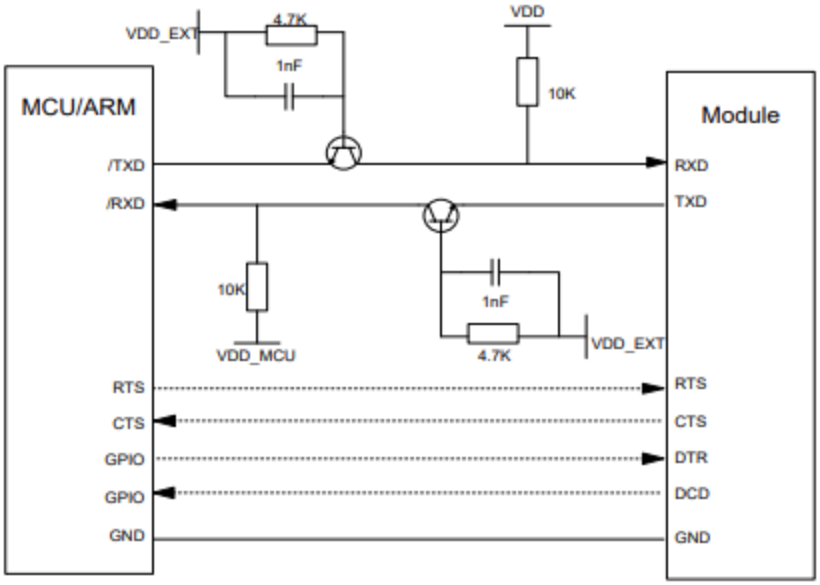

Figure 17-UART Signal Connection

3.10. Status Indication

The status indication pins are mainly used to drive network status indicator LEDs. The **E70x Series** module has two status indication pins: STATUS and NET_STATUS. The following two tables describe the pin definitions and the logic level changes under different network states.

Table 16- Status Indication Pin Description

Pin Name	I/O	Pin	Description
STATUS	DO	25	Module operating status indicator; outputs high level after the module is powered on
NET_STATUS	DO	16	Module network status indicator

Table 17- NET_STATUS Indicator Pin Working States

Pin Name	Pin Working State	Indicated Working State

NET_STATUS	Slow blink (200 ms high / 1800 ms low)	Network searching state
NET_STATUS	Slow blink (1800 ms high / 200 ms low)	Standby state
NET_STATUS	Fast blink (125 ms high / 125 ms low)	Data transmission mode
NET_STATUS	High level	In call

NET_STATUS is used to indicate the working status of the module network. The reference circuit is shown in the figure below:

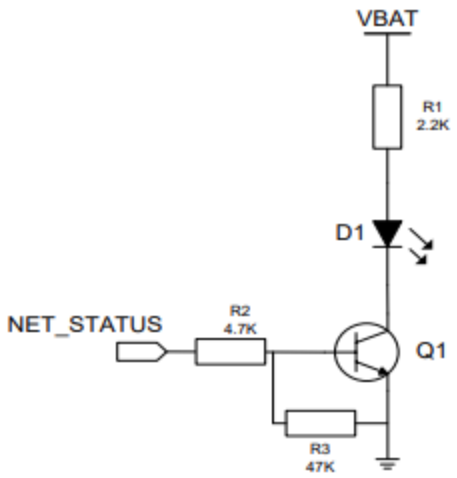

Figure 18-NET_STATUS Reference Circuit

STATUS is used to indicate the working status of the module. The reference circuit is shown in the figure below:

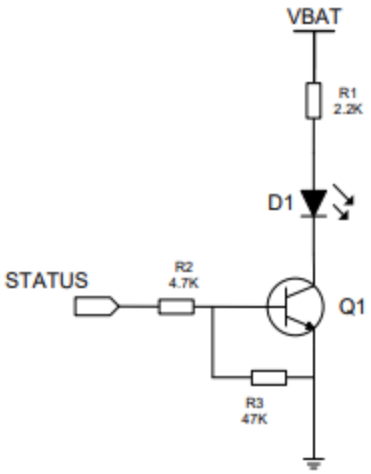

Figure 19-STATUS Reference Circuit

3.11. Low Power Mode

3.11.1. Flight Mode

The module supports entering flight mode using AT commands.

3.11.2. Ultra-Low Power Mode

The module supports entering ultra-low power mode using AT commands.

3.12. ADC Function

The **E70x Series** provides two 12-bit analog-to-digital conversion interfaces. The ADC voltage range is 0–1.2 V.

Table 18- ADC Pin Description

Pin Name	I/O	Pin	Description
ADC0	AI	9	ADC interface; connect a 1 kΩ resistor in series when used, leave floating when not used
ADC1	AI	96	ADC interface; connect a 1 kΩ resistor in series when used, leave floating when not used

Notes:

1. When VBAT is not powered, the ADC interface must not be directly connected to any input voltage.
2. It is recommended to use a voltage divider circuit as the ADC input.
3. It is recommended to apply ground shielding when routing the ADC pins to improve ADC voltage measurement accuracy.

3.13. USB_BOOT Interface

The **E70x Series** supports the USB_BOOT function. Customers can short USB_BOOT to ground before powering on the module, and then power it on. The module will enter forced download mode. In this mode, the module can perform software upgrades through the USB interface.

Table 19- USB_BOOT Pin Definition

Pin Name	I/O	Pin	Description
USB_BOOT	DI	82	Forced download mode, active low

3.14. I2C Interface

Table 20- I2C Pin Definition

Pin Name	I/O	Pin	Description
CI2C_SCL	OD	67	CI2C1 interface clock signal
CI2C_SDA	OD	66	CI2C1 interface data signal
I2C2_SCL	OD	68	I2C2 interface clock signal
I2C2_SDA	OD	69	I2C2 interface data signal

3.15. GPIO Interface

Table 21- GPIO Pin Definition

Pin Name	I/O	Pin	Description
GPIO_1 / PCM_CLK	I/O	30	General-purpose GPIO; configurable as PCM clock signal
GPIO_2 / PCM_SYNC	I/O	31	General-purpose GPIO; configurable as PCM frame sync
GPIO_3 / PCM_DIN	I/O	32	General-purpose GPIO; configurable as PCM data input
GPIO_4 / PCM_DOUT	I/O	33	General-purpose GPIO; configurable as PCM data output
GPIO_5	I/O	54	General-purpose GPIO
GPIO_6	I/O	55	General-purpose GPIO
GPIO_7	I/O	56	General-purpose GPIO

3.16. LCD Interface

Table 22- LCD Pin Definition

Pin Name	I/O	Pin	Description
LCD_RST	DO	49	LCD reset
LCD_SPI_DOUT	DO	50	LCD data output
LCD_SPI_RS	DO	51	LCD register select
LCD_SPI_CS	DO	52	LCD chip select
LCD_SPI_CLK	DO	53	LCD clock
LCD_TE	DI	78	LCD tearing effect

4. Antenna Interface

The **E70x Series** module is designed with two antenna interfaces. The antenna interface impedance is 50 Ω.

Table 23- Antenna Interface Pin Definition

Pin Name	Pin No.	Description	I/O	Remarks
ANT_MAIN	35	Main antenna / WIFI SCAN antenna interface	IO	50 Ω impedance
ANT_GNSS	2	GNSS antenna interface	IO	impedance

4.1. Antenna Interface Introduction

The **E70x Series** provides two antenna pins: ANT_MAIN and ANT_GNSS. Users are recommended to use antennas with 50 Ω impedance that match the RF connector on the module side.

Note:

To ensure communication capability across all frequency bands, it is recommended that the application side carefully select the RF adapter cable. An RF adapter cable with the lowest possible loss should be selected. The following RF insertion loss requirements are recommended for the RF adapter cable:

- TDD-LTE < 1.2 dB;
- FDD-LTE < 1.2 dB;

Recommended RF connectors:

Product name		MHF®4L LK	MHF®4L	MHF®4L	MHF®4L	MHF®4
Appearance						
		MHF 4L with Mechanical lock	Best Insertion Loss and VSWR	Industry Standard for M.2	Industry Standard for M.2	low profile1.20 mm
Plug part number		-	20632-001R-37	20565-001R-13	20572-001R-08	20611-001R
Receptacle part number		20449-001E-**(MHF 4) 20579-001E(MHF 4L)				
Maximum height (mm)		2.0	1.7	1.4	1.2	1.2
Outside dimension of receptacle (mm)		2.0 x 2.0				
Coax O.D. (Center Conductor AWG)	2.00 mm (26)					
	1.80 mm (30)					
	1.37 mm (30)	●	●			
	1.32 mm (32)					
	1.13 mm (32)			●		
	0.95 mm (33)			●		
	0.81 mm (33)					
	0.81 mm (36)				●	●
	0.64 mm (36)				●	
	0.48 mm (38)					
Frequency		DC - 12 GHz				DC - 6 GHz
VSWR (L=100mm)	DC - 3 GHz	1.3 max.				
	3 GHz - 6 GHz	1.4 max.		1.45 max		1.5 max.
	6 GHz - 9 GHz	1.5 max.		1.6 max.		-
	9 GHz - 12 GHz	1.6 max.		1.9 max.		-
	12 GHz - 15 GHz	-				
Service temp. (Celsius)		-40 degree - 90 degree				
Characteristic impedance		50ohm				
Rated voltage		AC60V				
Contact resistance		20m ohm max.				
Withstand voltage		AC200V/min				
Insulation resistance		500M ohm min./DC100V				

Figure 20-RF Connector

4.2. RF Reference Circuit

4.2.1. Antenna Connection Reference Design

The reference design circuit for the ANT_MAIN antenna connection is shown in the figure below. To obtain better RF performance, the following four points should be noted during schematic design and PCB layout:

1. In schematic design, reserve a π-type matching circuit close to the module RF port; capacitors are not populated by default;
2. In schematic design, reserve an RF connector between the module RF port and the antenna for certification testing; after mass production shipment, the RF connector does not need to be populated (reference: RF connector C88P132-00001-H);
3. In schematic design, reserve a π-type matching circuit close to the antenna side; capacitors are not populated by default;
4. In PCB layout, the routing between the module RF port and the antenna should be as short as possible, and the PCB manufacturer must perform 50 Ω impedance control on the RF routing.

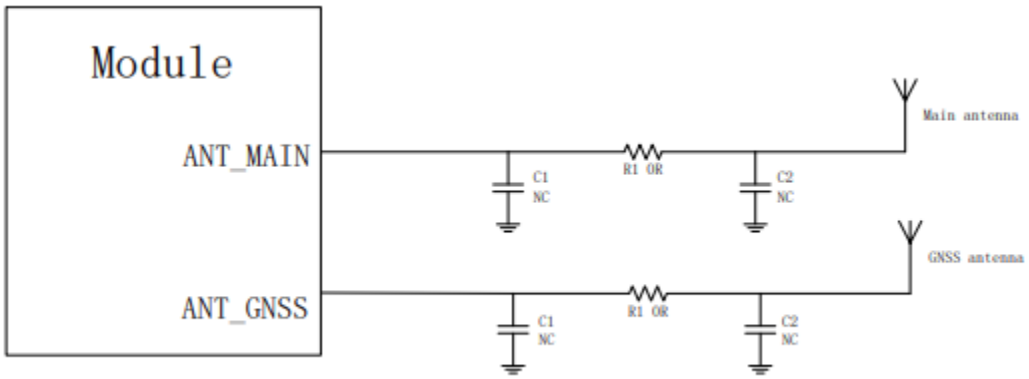

Figure 21-RF Reference Circuit

4.2.2. RF Signal Routing Guidelines

For user PCBs, the characteristic impedance of all RF signal traces should be controlled at 50 Ω. Generally, the impedance of RF signal traces is determined by the dielectric constant of the material, trace width (W), clearance to ground (S), and the height of the reference ground plane (H). PCB characteristic impedance control usually adopts microstrip and coplanar waveguide structures. To illustrate the design principles, the following figures show the structural designs of microstrip and coplanar waveguide when the impedance is controlled at 50 Ω.

- Complete microstrip structure

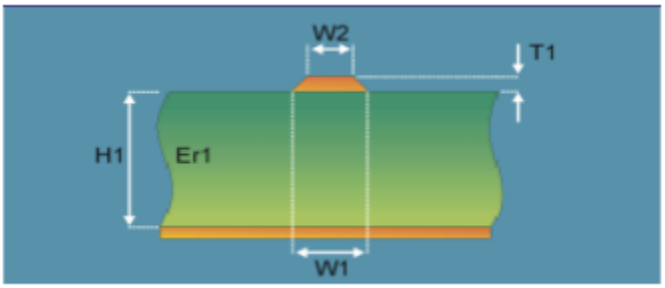

Figure 22-Two-Layer PCB Microstrip Line Structure

- Complete coplanar waveguide structure

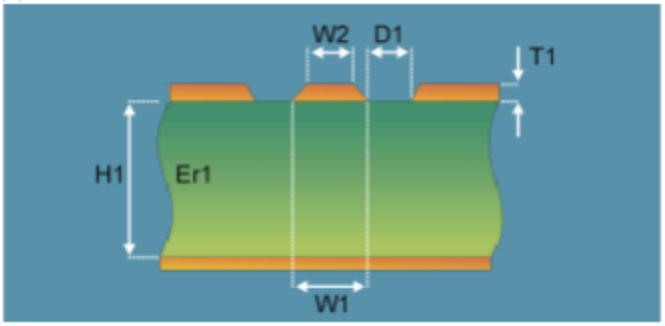

Figure 23-Two-Layer PCB Coplanar Waveguide Structure

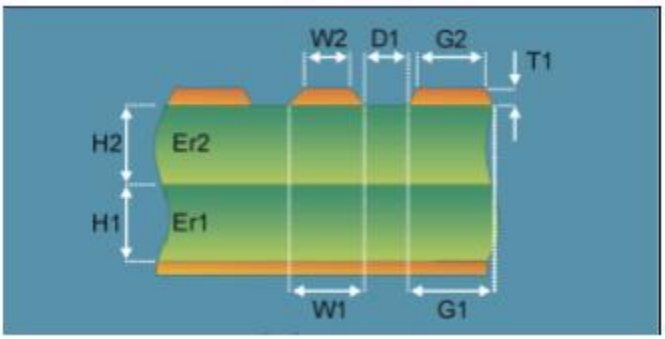

Figure 24-Multilayer PCB Coplanar Waveguide Structure (Reference Ground on Layer 3)

Note:

W1: maximum trace width
W2: minimum trace width
T1: copper thickness
H1: board dielectric thickness
ERI: board dielectric constant

In the RF antenna interface circuit design, in order to ensure good RF signal performance and reliability, it is recommended to follow the design principles below:

- Use impedance simulation calculation tools to accurately control the RF signal trace impedance to 50 Ω;
- Do not use thermal relief pads for GND pins adjacent to RF pins; ensure full contact with ground;
- Keep the distance between the RF pin and the RF connector as short as possible; avoid right-angle routing, and the recommended routing angle is 135°;
- Pay attention when creating component footprints to ensure that the signal pin maintains a certain distance from ground;
- The ground plane referenced by RF signal traces should be complete; adding a certain number of ground vias around the signal trace and reference ground can help improve RF

performance; the distance between ground vias and signal traces should be at least twice the trace width (2 × W);

- RF signal traces must be kept away from interference sources and must avoid crossing or running in parallel with any signal traces on adjacent layers.

4.3. Antenna Installation

4.3.1. Antenna Requirements

The requirements for the antenna are shown in the table below:

Table 24- Antenna Requirements

Type	Requirement
TDD-LTE / FDD-LTE	VSWR: < 2
	Gain (dBi): 1
	Maximum input power (W): 2 W
	Input impedance (ohm): 50
	Polarization type: vertical
	Cable insertion loss: < 1.5 dB (LTE B1/B3/B5/B8/B34/B39)
	Cable insertion loss: < 2 dB (LTE B38/B40/B41)

4.3.2. RF Output Power

The RF output power of the **E70x Series** is shown in the table below.

Table 25- E70x Series RF Transmit Power

Frequency	Maximum	Minimum
LTE-FDD B1	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-FDD B3	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-FDD B5	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-FDD B8	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-TDD B34	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-TDD B38	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-TDD B39	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-TDD B40	**23 dBm ± 2.7 dB**	**< -39 dBm**
LTE-TDD B41	**23 dBm ± 2.7 dB**	**< -39 dBm**

4.3.3. RF Receive Sensitivity

Table 26- E70x Series Module RF Receive Sensitivity

Frequency	Receive Sensitivity (Typical, BW = 10 MHz)
	Main
LTE-FDD B1	-97 dBm
LTE-FDD B3	-97 dBm
LTE-FDD B5	-98 dBm

LTE-FDD B8	-98 dBm
LTE-TDD B34	-97.5 dBm
LTE-TDD B38	-97.5 dBm
LTE-TDD B39	-97.5 dBm

Note:
Information on other sub-models and frequency bands will be reflected in subsequent versions of this document.

4.3.4. Operating Frequency

Table 27- E70x Series Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE-FDD B1	**1920–1980**	**2110–2170**	**MHz**
LTE-FDD B3	**1710–1785**	**1805–1880**	**MHz**
LTE-FDD B5	**824–849**	**869–894**	**MHz**
LTE-FDD B8	**880–915**	**925–960**	**MHz**
LTE-TDD B34	**2010–2025**	**2010–2025**	**MHz**

LTE-TDD B38	**2570–2620**	**2570–2620**	**MHz**
LTE-TDD B39	**1880–1920**	**1880–1920**	**MHz**
LTE-TDD B40	**2300–2400**	**2300–2400**	**MHz**
LTE-TDD B41	**2540–2650**	**2540–2650**	**MHz**

4.3.5. OTA Antenna Requirements

Table 28- Antenna Performance Requirements

Network Mode	Band	VSWR	Gain	Effi.	SAR	TRP (dBm) Peak	TIS (dBm) Avg.
TDD-LTE	Band34	< 2.5:1	> 0 dBi	> -4 dBi	> 40%	< 1.6 W/Kg	19
	Band38					19	< -92
	Band39					19	< -92
	Band40					19	< -92
	Band41					19	< -92
FDD-LTE	Band1					19	< -92
	Band3					19	< -92
	Band5					19	
	Band8					19	< -92

5. Electrical Characteristics

5.1. Absolute Maximum Voltage Range

The absolute maximum voltage range refers to the maximum voltage range that the module power supply voltage and the digital and analog input/output interfaces can withstand. Operation outside this range may cause damage to this product.

The absolute maximum voltage range of the **E70x Series** is shown in the table below.

Table 29- Module Absolute Maximum Operating Voltage Range

Parameter	Description	Minimum	Typical	Maximum	Unit
VBAT	Power supply	-0.3	3.8	5.5	V
GPIO	Digital I/O level supply voltage	-0.3	1.8	2.0	V
VBUS	USB insertion detection	-0.3	5.0	5.5	V

5.2. Ambient Temperature Range

The **E70x Series** module is recommended to operate in an environment of -35 to +75 °C. It is recommended that the application side consider temperature control measures under harsh environmental conditions. An extended operating temperature range is also provided for the module. When used in the extended temperature range, functionality is normal, but some RF specifications may degrade. It is also recommended that the module application terminal store the module within a certain temperature range. Outside this range, the module may not operate normally or may be damaged.

Table 30- Module Temperature Range

Pin Name	Pin No.	Description	I/O	Remarks

Operating temperature	-35	+25	+75	°C
Storage temperature	-40		+85	°C

5.3. Electrical Characteristics of Interface Operating States

VL: logic low level; VH: logic high level.

Table 31- Logic Levels of General Digital IO Signals

Signal	VL	VH	Unit
	Minimum	Maximum	Minimum
Digital input	-0.3	0.36	1.26
Digital output		0.45	1.35

Table 32- Electrical Characteristics of Power Supply Operating States

Parameter	I/O	Minimum	Typical	Maximum	Unit
VBAT	PI	3.5	3.8	4.2	V
USIM_VDD	PO	1.62 / 2.7	1.8 / 3.0	1.9 / 3.3	V
VBUS	AI	4.5	5.0	5.5	V

5.4. Module Power Consumption Range

Table 33- Power Consumption

Module State	Test Item	Test Case	Result
Power off	Power-off leakage current	Maintain normal voltage (3.8 V) supply when powered off	TBD
sleep mode	Flight sleep mode	Enable flight mode and sleep using AT commands, record the average current over 10 minutes	TBD
	PSM	Refer to PSM test documentation	TBD
	Live network sleep	Insert China Mobile SIM, actual network standby, enable sleep mode via AT commands, record the average current over 5 minutes	TBD
		Insert China Unicom SIM, actual network standby, enable sleep mode via AT commands, record the average current over 5 minutes	TBD
		Insert China Telecom SIM, actual network standby, enable sleep mode via AT commands, record the average current over 5 minutes	TBD
		Insert China Mobile SIM, module sleeps after receiving SMS on live network, record the average current over 5 minutes	TBD
		Maintain data connection, send a 256-byte data packet every 5 minutes, server returns	TBD

			a 256-byte data packet	
	FDD	Module powered on, registered to network idle state; DRX listening cycle is 1.28 s; 1) Power on and successfully register to data network; 2) Set module to sleep state via AT commands (USB in suspend state); 3) Maintain no data transmission for 10 minutes, record the average current over 10 minutes	Band1 CH18300	TBD
			Band3 CH19575	TBD
			Band5 CH20525	TBD
			Band8 CH21625	TBD
	TDD		Band34 CH36275	TBD
			Band38 CH38000	TBD
			Band39 CH38450	TBD
			Band40 CH39150	TBD
			Band41 CH40620	TBD
Standby	FDD	Module powered on, registered to network idle state; DRX listening cycle is 1.28 s; no data transmission, USB in active state; maintain no data transmission for 10 minutes and record the average current	Band1 CH18300	TBD
			Band3 CH19575	TBD
			Band5 CH20600	TBD
			Band8 CH21750	TBD
	TDD		Band34 CH36275	TBD
			Band38 CH38000	TBD
			Band39 CH38450	TBD
			Band40 CH39150	TBD
			Band41 CH40620	TBD
Data transmission	FDD		Band1 0 dBm	TBD
			Band1 10 dBm	TBD
			Band1 23 dBm Low channel	TBD
			Band1 23 dBm Middle channel	TBD
			Band1 23 dBm High channel	TBD
			Band3 0 dBm	TBD

		1) Indoor room temperature; 2) Module powered by DC power supply set to 3.8 V; module performs data transmission and maintains for 5 minutes, record the average current over 5 minutes	Band3 10 dBm	TBD
			Band3 23 dBm Low channel	TBD
			Band3 23 dBm Middle channel	TBD
			Band3 23 dBm High channel	TBD
			Band5 0 dBm	TBD
			Band5 10 dBm	TBD
			Band5 23 dBm Low channel	TBD
			Band5 23 dBm Middle channel	TBD
			Band5 23 dBm High channel	TBD
			Band8 0 dBm	TBD
			Band8 10 dBm	TBD
			Band8 23 dBm Low channel	TBD
			Band8 23 dBm Middle channel	TBD
			Band8 23 dBm High channel	TBD
	TDD		Band34 0 dBm	TBD
			Band34 10 dBm	TBD
			Band34 23 dBm Low channel	TBD
			Band34 23 dBm Middle channel	TBD
			Band34 23 dBm High channel	TBD
			Band38 0 dBm	TBD
			Band38 10 dBm	TBD
			Band38 23 dBm Low channel	TBD
			Band38 23 dBm Middle channel	TBD
			Band38 23 dBm High channel	TBD
			Band39 0 dBm	TBD
			Band39 10 dBm	TBD

			Band39 23 dBm Low channel	TBD
			Band39 23 dBm Middle channel	TBD
			Band39 23 dBm High channel	TBD
			Band40 0 dBm	TBD
			Band40 10 dBm	TBD
			Band40 23 dBm Low channel	TBD
			Band40 23 dBm Middle channel	TBD
			Band40 23dBm High channel	TBD
			Band41 0dBm	TBD
			Band41 10dBm	TBD
			Band41 23dBm Low channel	TBD
			Band41 23dBm Middle channel	TBD
			Band41 23dBm High channel	TBD

5.5. ESD Characteristics

The module does not have dedicated protection against electrostatic discharge. Therefore, users must pay attention to ESD protection during production, assembly, and operation of the module.

6. Mechanical Characteristics

This chapter describes the mechanical dimensions of the module. All dimensions are in millimeters. For all dimensions without specified tolerances, the tolerance is ±0.05 mm.

6.1. Module Mechanical Dimensions

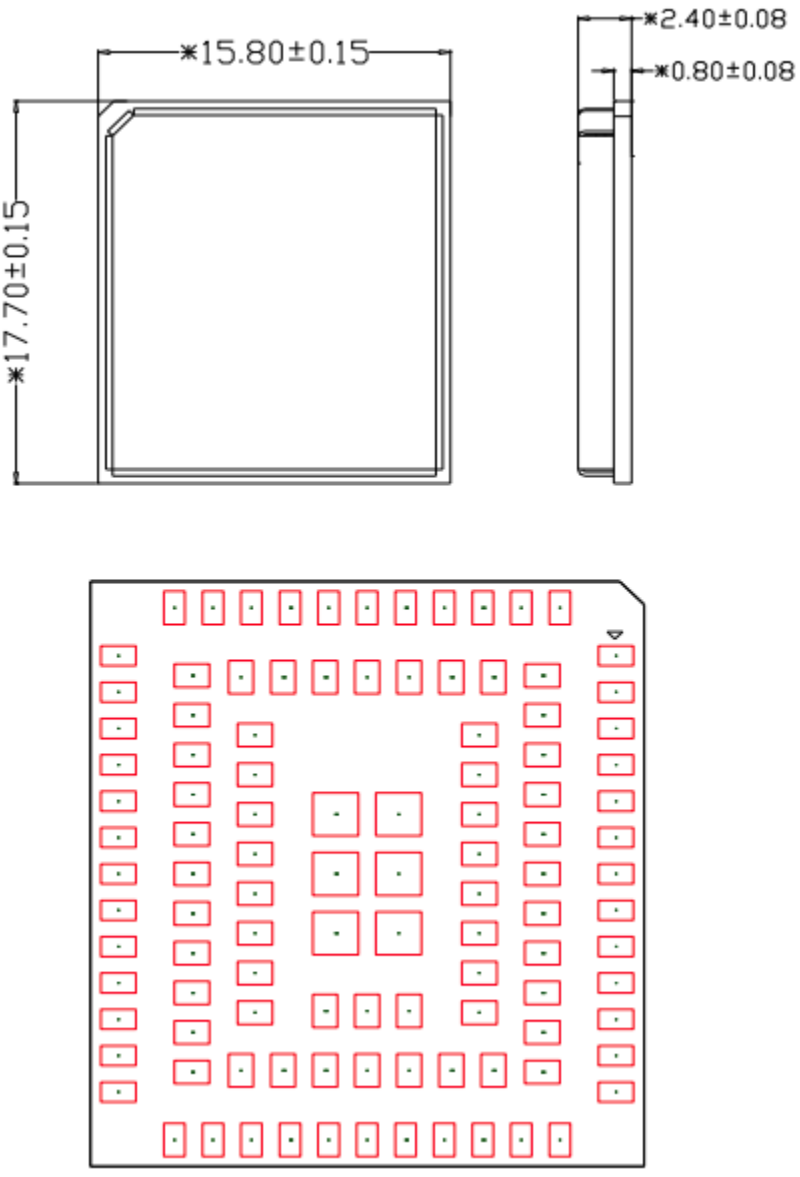

Figure 25-Top View and Bottom View

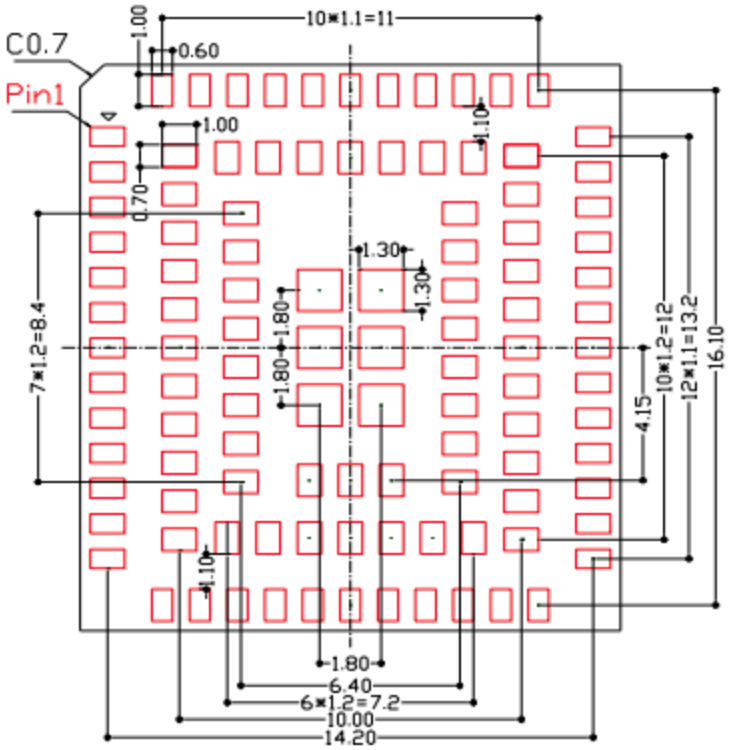

Figure 26-Recommended Package Dimensions (Unit: mm)

6.2. Module Top View

Figure 27-Module Top View

6.3. Module Bottom View

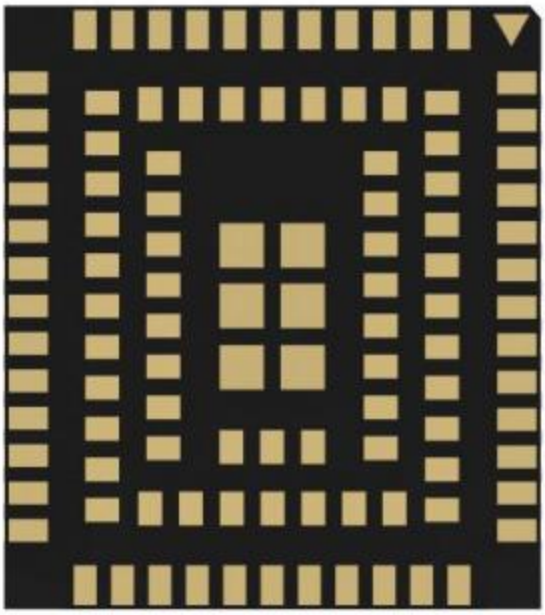

Figure 28-Module Bottom View

7. Storage and Packaging

7.1. Storage

The **E70x Series** is shipped in vacuum-sealed bags. Module storage must comply with the following conditions:

1. When the ambient temperature is below 40 °C and the air humidity is less than 90%, the module can be stored in the vacuum-sealed bag for 12 months.
2. After the vacuum-sealed bag is opened, if the following conditions are met, the module can directly undergo reflow soldering or other high-temperature processes:
    - The storage air humidity of the module is less than 10%;
    - The ambient temperature of the module is below 30 °C, the air humidity is less than 60%, and SMT is completed within 72 hours.
3. If the module is under the following conditions, baking is required before SMT:
    - When the ambient temperature is 23 °C (±5 °C allowed), and the humidity indicator shows humidity greater than 10%;
    - After opening the vacuum-sealed bag, the module ambient temperature is below 30 °C and the air humidity is less than 60%, but SMT is not completed within 168 hours;
    - After opening the vacuum-sealed bag, the module storage air humidity is greater than 10%.
4. If baking is required, bake the module at 125 °C (±5 °C allowed) for 8 hours.

Note:
The module packaging cannot withstand such high temperatures. Remove the packaging before baking the module.

7.2. Production Soldering

Note:
The above oven temperature profile is for reference only. Customers may optimize it according to the actual product characteristics.

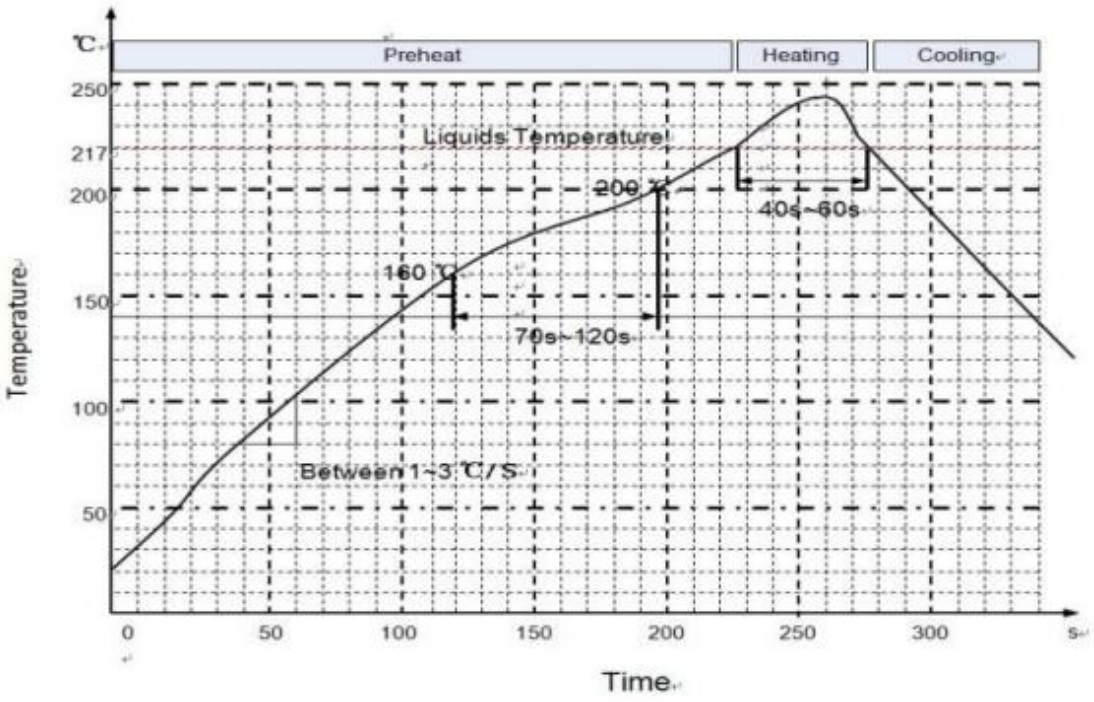

Figure 29-Reflow Oven Temperature Profile and Lead-Free Reflow Temperature Reference Parameters

Table 34-Temperature Reference Parameters

Parameter	Value
Preheating temperature rise requirement (<160°C)	≤2°C/s
Average ramp rate (165°C to 217°C)	60~100s
Peak temperature rise rate	1~3°C/s
Minimum temperature at peak	230°C
Maximum temperature at peak	250°C
Time above liquidus (≥217°C)	35~90s

Time above 230°C	**٢٥~50 s**
Cooling rate (T=217~120°C)	**-2~-5°C/s**
Maximum slope during cooling	**-6°C/s**
Time from 50°C to 217°C	**150~240s**
Number of reflow zones	**≥7**

Note:
The calculation of the maximum temperature slope should be based on a minimum interval of 10 s. Shorter intervals may cause errors, especially for small components or components with low thermal mass, resulting in large slope values. The above parameters are based on average board temperature. Single-point peak temperature and liquidus temperature at the peak point must also meet requirements.

7.3. Packaging

The **E70x Series** uses tape-and-reel packaging.

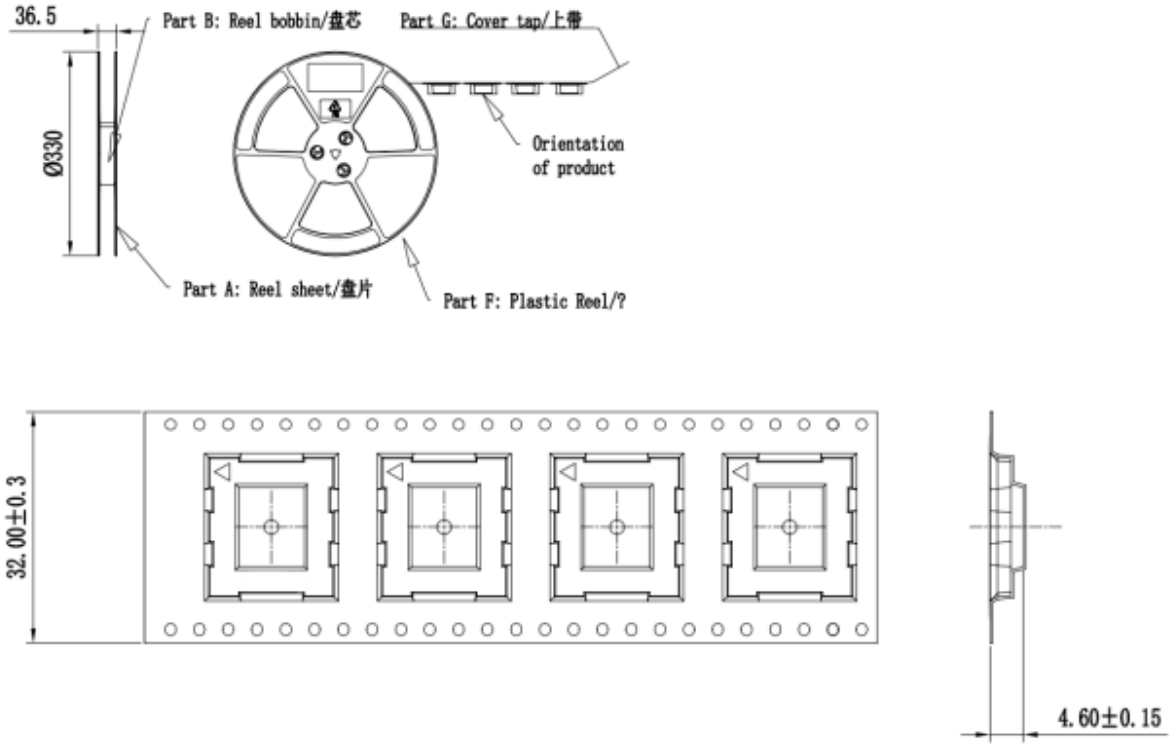

Figure 30-Tape-and-Reel Packaging

8. Appendix A: Reference Documents and Abbreviations

8.1. Reference Documents

- **E70x Series** Module Specification
- **E70x Series** AT Command Set
- **E70x Series** Reference Design Circuit
- **E70x Series** Application Process Manual

8.2. Abbreviations

Abbreviation	English Description
AMR	Adaptive Multi-rate
BER	Bit Error Rate
BTS	Base Transceiver Station
PCI	Peripheral Component Interconnect
CS	Circuit Switched (CS) domain
CSD	Circuit Switched Data
DCE	Data communication equipment
DTE	Data terminal equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

EMC	**Electromagnetic Compatibility**
ESD	**Electrostatic Discharge**
FR	**Frame Relay**
GMSK	**Gaussian Minimum Shift Keying**
GPIO	**General Purpose Input Output**
GPRS	**General Packet Radio Service**
GSM	**Global Standard for Mobile Communications**
HR	**Half Rate**
HSDPA	**High Speed Downlink Packet Access**
HSUPA	**High Speed Uplink Packet Access**
HSPA	**High-Speed Packet Access**
HSPA+	**High-Speed Packet Access+**
IEC	**International Electro-technical Commission**
IMEI	**International Mobile Equipment Identity**
MEID	**Mobile Equipment Identifier**
I/O	**Input/Output**
ISO	**International Standards Organization**
ITU	**International Telecommunications Union**
bps	**bits per second**
LED	**Light Emitting Diode**

M2M	**Machine to machine**
MO	**Mobile Originated**
MT	**Mobile Terminated**
NTC	**Negative Temperature Coefficient**
PC	**Personal Computer**
PCB	**Printed Circuit Board**
PCS	**Personal Cellular System**
SPI_FLASH	**Pulse Code Modulation**
PCS	**Personal Communication System GSM1900**
PDU	**Packet Data Unit**
PPP	**Point-to-point protocol**
PS	**Packet Switched**
QPSK	**Quadrate Phase Shift Keying**
SIM	**Subscriber Identity Module**
TCP/IP	**Transmission Control Protocol / Internet Protocol**
UART	**Universal asynchronous receiver-transmitter**
SIM	**Universal Subscriber Identity Module**
UMTS	**Universal Mobile Telecommunications System**
USB	**Universal Serial Bus**
WCDMA	**Wideband Code Division Multiple Access**

TD-SCDMA	**Time Division-Synchronous Code Division Multiple Access**
TDD-LTE	**Time Division Long Term Evolution**
FDD-LTE	**Frequency Division Duplexing Long Term Evolution**
Vmax	**Maximum Voltage Value**
Vnorm	**Normal Voltage Value**
Vmin	**Minimum Voltage Value**
VIHmax	**Maximum Input High Level Voltage Value**
VIHmin	**Minimum Input High Level Voltage Value**
VILmax	**Maximum Input Low Level Voltage Value**
VILmin	**Minimum Input Low Level Voltage Value**
VOHmax	**Maximum Output High Level Voltage Value**
VOHmin	**Minimum Output High Level Voltage Value**
VOLmax	**Maximum Output Low Level Voltage Value**
VOLmin	**Minimum Output Low Level Voltage Value**